High Density Motor Drive for More-Electric Aircraft

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Project Overview  Hardware Progress
Outline

Project Overview

Technical Strategy

Hardware Progress

Next Steps
Overview and Motivation

- Hybrid flight promises to provide significant benefits including fuel savings, reduced noise, and reduced CO$_2$ emissions.
- Power specific density is a key limitation in the pursuit of more-electric flight [1].
- Improvements in density will require integrated electrical, mechanical, and thermal design

Overview and Motivation

Final Goal: 1 MW, non-cryogenic PM machine with integrated drive.

- Objective power density of ~10 kW/kg for co-designed system.
- Enabling technology for estimated 63% reduction in fuel burn in Boeing 737 equivalent aircraft at 1000 mile range with 22 db noise reduction.
Drive Architecture - Overview

- Parallel architecture enables:
  - Higher reliability
  - Better thermal management
    - Distributed losses
    - Higher light-load efficiency
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Drive Architecture - Overview

- Flying capacitor multilevel inverter used (FCML).
- Overall 1 MW inverter divided into ~30 smaller inverters (10/phase)
- 1 kV center-tapped DC bus
- Each phase consists of 20 windings
  Grouped in sets of 2 series coils
Each inverter supplies ~92 A at 360 $V_{rms}$
13 Level FCML Inverter Prototype

- **Design Goals**
  - 13-level flying capacitor
  - 6 kW design
    - 1 kV dc input
    - $17 \text{ A}_{\text{RMS}}/360 \text{ V}_{\text{RMS}}$ output

- **Learning Opportunities**
  - Layout at 1 kV
  - Scaling measurement setup to high power
  - Passive & active control of 13-level topology
  - Understanding of component performance at high frequency (capacitors and inductors).
FCML Overview

- Switches $S_{Na}$ and $S_{Nb}$ are complementary.
- Only one transition is needed between states.
- Frequency seen by inductor is $F_{\text{switch}} \times (N-1)$.

\[
c_2 = \frac{2V_{\text{in}}}{3} \quad c_1 = \frac{V_{\text{in}}}{3}
\]

Config B2: $V_{\text{out}} = \frac{V_{\text{in}}}{3}$

Config B3: $V_{\text{out}} = \frac{V_{\text{in}}}{3}$

Config A1: $V_{\text{out}} = 0$

Relationship between $V_L$ and switch transitions
FCML Overview

- Capacitors balanced by choice of switch configuration
- Ideally, voltage measurements are not needed.

\[
c_2 = \frac{2V_{in}}{3} \quad c_1 = \frac{V_{in}}{3}
\]

Step 1

Step 2

Step 3
Power Electronics - Improved Switching Cell

\[ L_{par1} \gg L_{par2} \gg L_{par3} \]

Version 1

Version 2

Version 3
Power Electronics - Improved Switching Cell

$L_{par1} \gg L_{par2} \gg L_{par3}$

Version 1

Version 3
Relationship Between $R_{DS\_On}$ & Device Temperature

- Maximum thermal limits and cooling capability define a usable device rating
- Measured $R_{DS\_On}$ as an indicator of device temperature
  - $R_{DS\_On}$ determined through high accuracy voltage drop and current measurements
- Calibration of this $R_{DS\_On}$ measurement needed for absolute temperature measurement
- Measurements agree with manufacturer datasheet
Theoretical Calculation of Thermal Impedance

- Thermal impedance from junction to case is known
  \[ R_{JC-Device} = 0.45 \frac{K}{W} \]

- Thermal impedance from GaN to heat sink can be calculated (Note: Gap-Pad Bergquist GP5000S35)
  \[
  R_{Gap} = R_{GapPad} \times \frac{d_{GaN-to-Heatsink}}{A_{GaN}}
  \]
  \[
  R_{Gap} = 0.125 \left[ \frac{m-K}{W} \right] \times \frac{0.45[mm]}{30[\mu m^2]} = 3.3 \frac{K}{W}
  \]

- Thermal impedance of junction to heat sink
  \[ R_{J-Sink} = R_{Gap} + R_{JC-Device} = 3.75 \frac{K}{W} \]
Experimental Evaluation of Thermal Impedance

- Using $R_{DS_{\text{On}}}$, junction temperature was evaluated for varying applied dc currents
- Thermal transfer to heat sink calculated based on measured losses and GaN junction temperature
- Measured data substantiates calculated thermal impedance of 3.75 [K/W]
- This thermal analysis establishes useable range for switch operation

Note: Lower power measurements are more susceptible to noise
13 Level FCML Inverter Prototype - Testing

- Daughter boards are functionally tested, but stress testing is challenging because of heatsinking requirements.
- Soldering daughter boards adds uncertainty as to how the device will perform.
- By adding additional jumper connections, each daughter board can be tested at rated voltage and current after it has been soldered in place.
Outline

1. Project Overview
2. Technical Strategy
3. Hardware Progress
4. Next Steps
13 Level FCML Inverter Prototype - Control

Integrated switching cell composed of 4 switches

Multiplied effective output frequency.

Single switch gate signal

Switch signal (phase 1)

Switch signal (phase 12)
FPGA-Based Control

- Intersecting capacitor voltages causes distortion in output current

- Greater control over changing duty ratio for all phases eliminates this problem
Low Power Test of 13-Level Inverter

- Inverter test results at partial load.
  - 600 W, THD = 0.8%, & Light-Load Efficiency = 94.8%
  - Losses are distributed in the inverter
  - Very low THD in output current waveform (4 $\mu$H inductor)

Thermal image of inverter

Inverter output waveform
• FPGA-based control has proven to generate very stable PWM.
  • Flying capacitors are well balanced.
  • Existing results show the feasibility of scaling up number of inverter levels.

When tested at partial bus voltage, capacitors are stable at increments of \( \frac{m \cdot V_{DC}}{N-1} \) volts where \( N \) is the number of levels and \( m \) increments from 1 to \( N-2 \).

Plot of inverter flying cap voltages.
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Next Steps for 13 Level Inverter

- Raise operating power.
  - Proper heatsink contact.
  - Incrementally test system to raise to full operating power

Inverter with FPGA and heatsink
Questions?