A 94.2%-Peak-Efficiency 1.53A Direct-Battery-Hook-Up Hybrid Dickson Switched-Capacitor DC-DC Converter with Wide Continuous Conversion Ratio in 65nm CMOS

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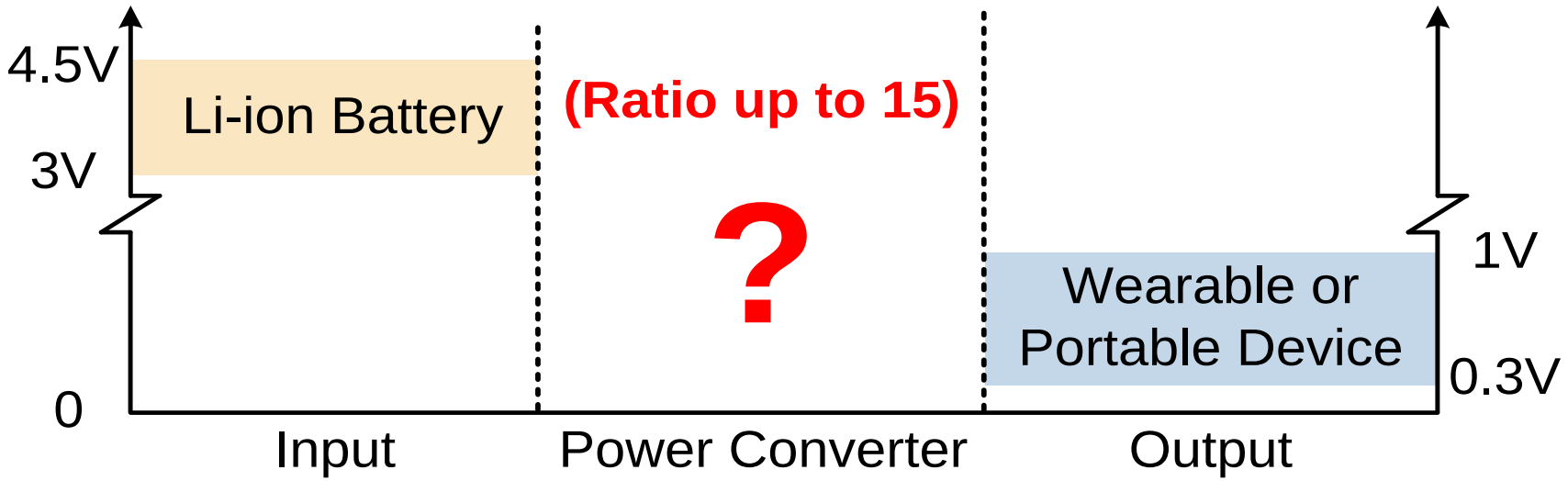
Motivation

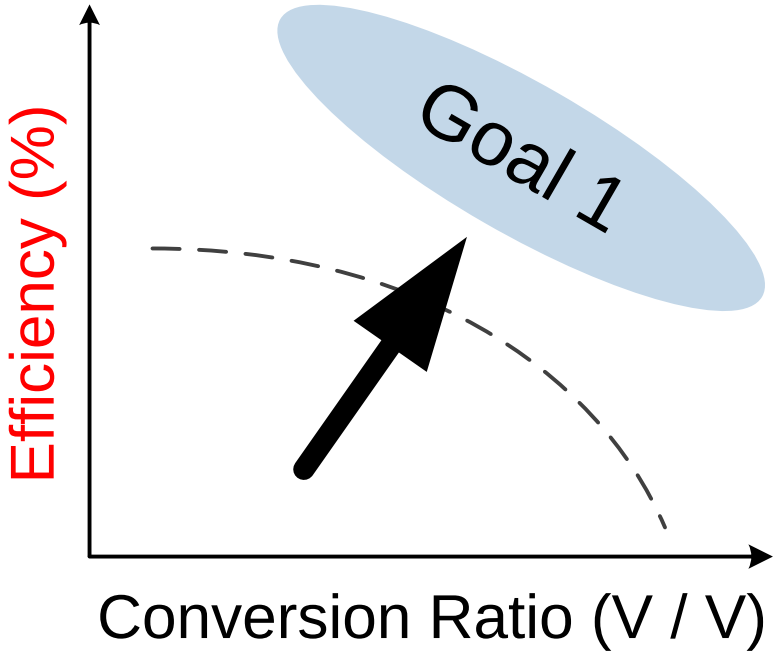
- Power converter requires
  - High conversion ratio
  - High current / power density
  - High efficiency

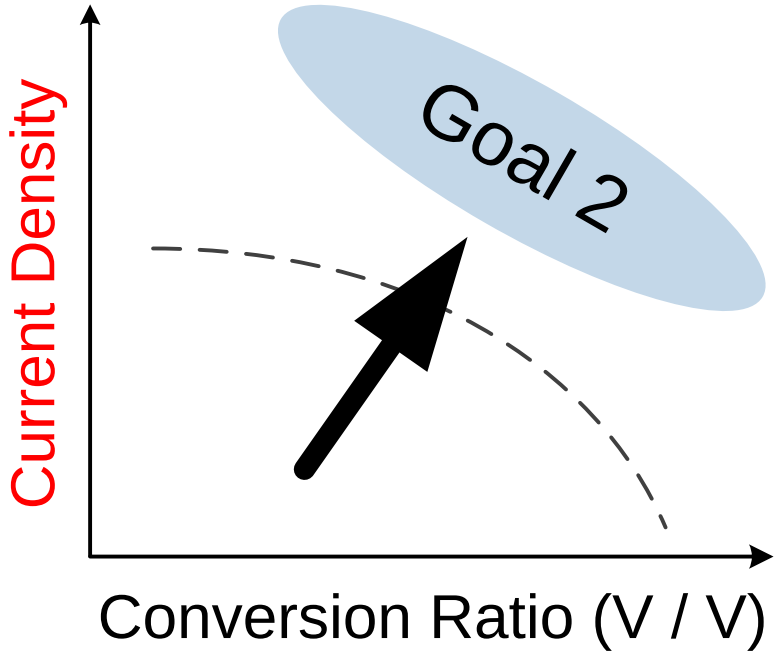
} WIDE-range regulation



Performance Index

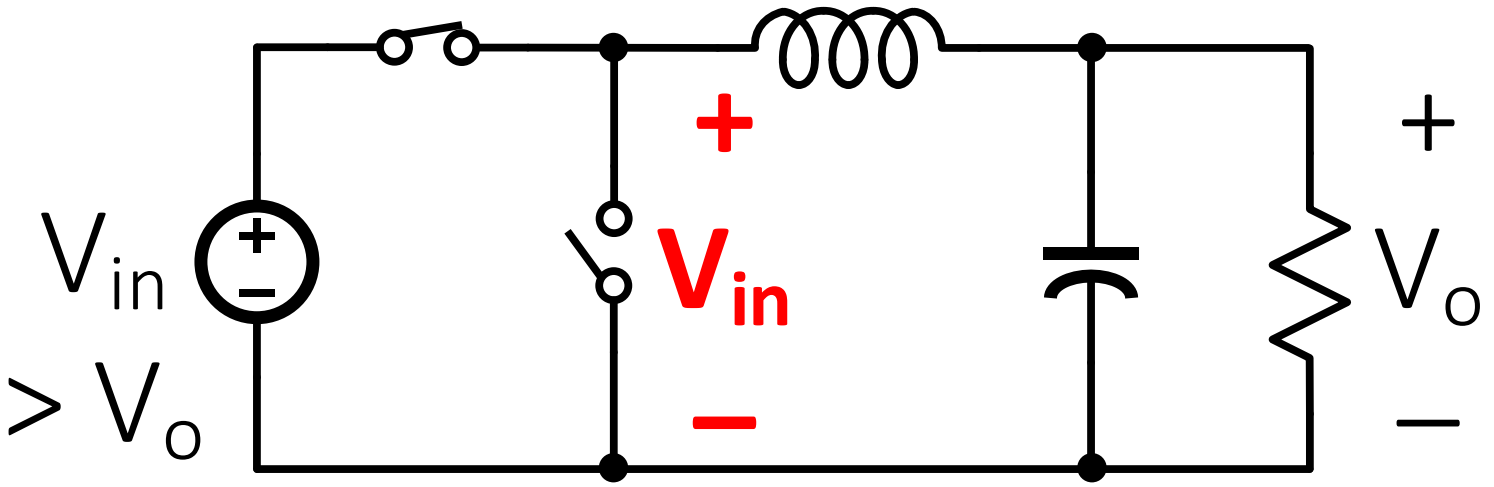
- Conventional SC converter
  - Goal 1 but only at some discrete high ratios
  - Prior arts addressed it using multiple stages but at the sacrifice of Goal 2





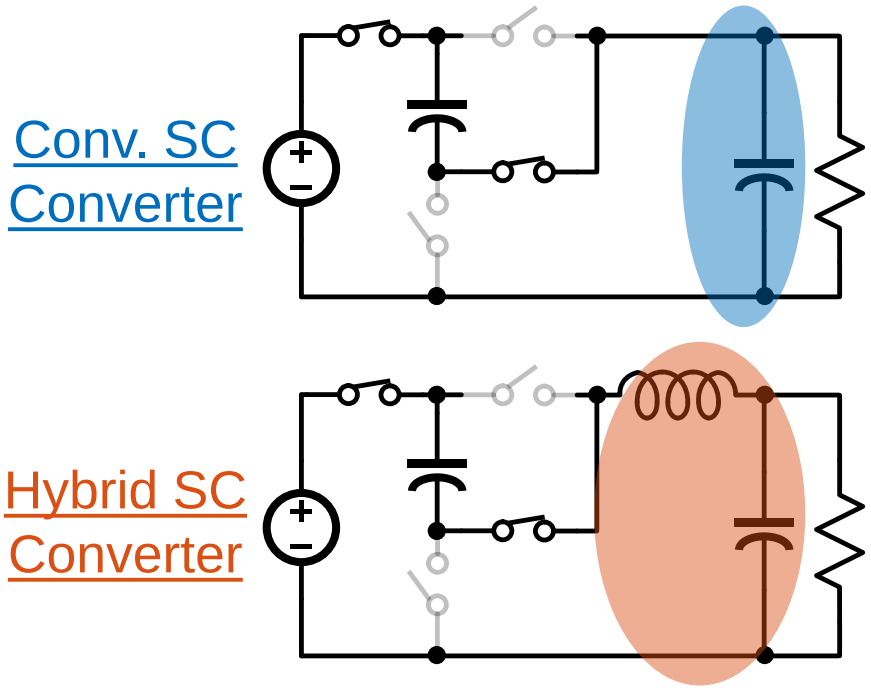
Performance Index

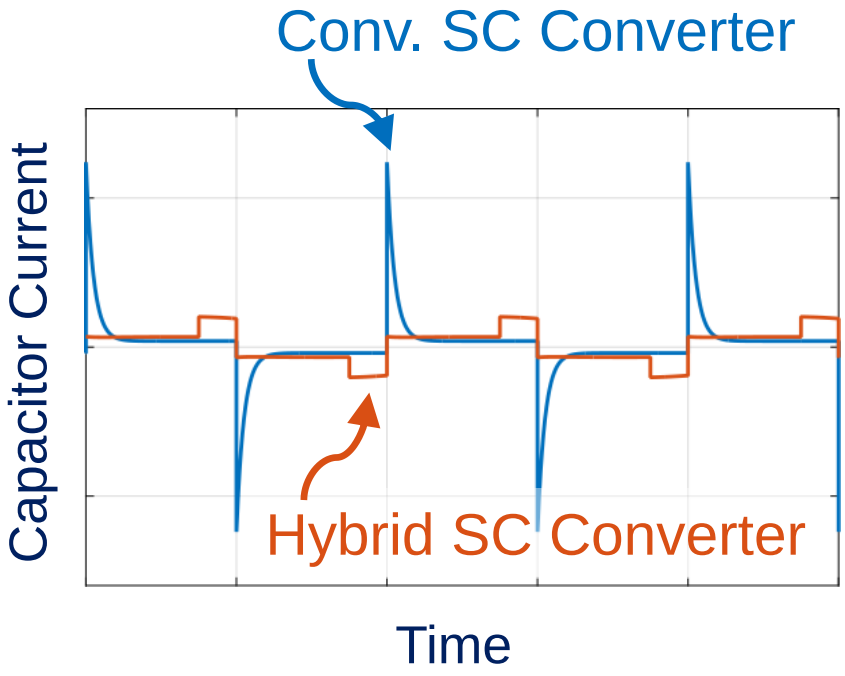
- Conventional buck converters
  - Hard to achieve Goals 1 and 2, due to the large device voltage stress relative to the output
  - High voltage rating: higher $R_{ds,on}$ per area



Hybrid SC Converter

- No more charge redistribution loss
  - Reduces the RMS and peak capacitor current
  - Low R_o and independent of switching frequency



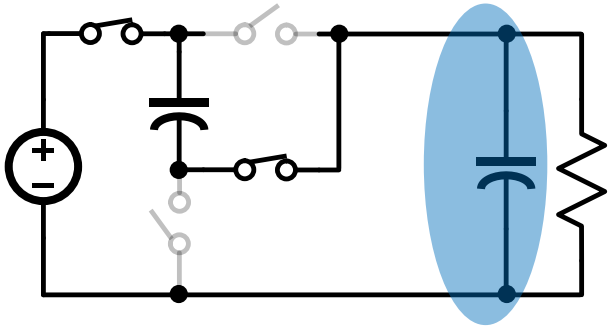


M. Seeman and S. Sanders, “Analysis and optimization of switched-capacitor dc-dc converters,” *IEEE Trans. Power Electron*., vol. 23, no. 2, pp. 841–851, Mar. 2008.

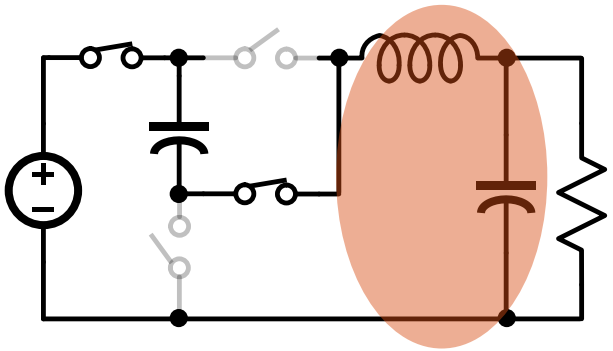
Hybrid SC Converter

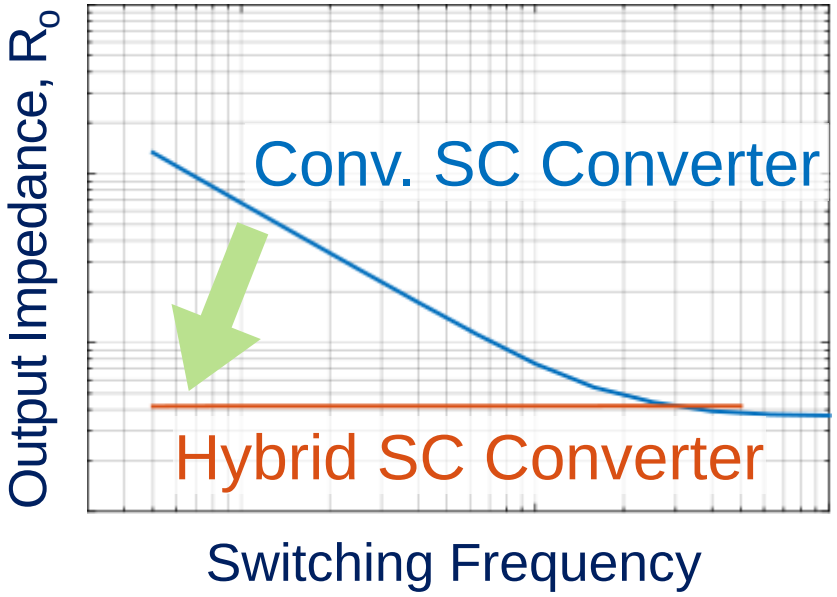
- Efficiency improvement
  - Larger capacitors voltage ripple is allowed
  - Capacitor values can be reduced
  - f_{sw} can be lowered to reduce switching losses

Conv. SC Converter



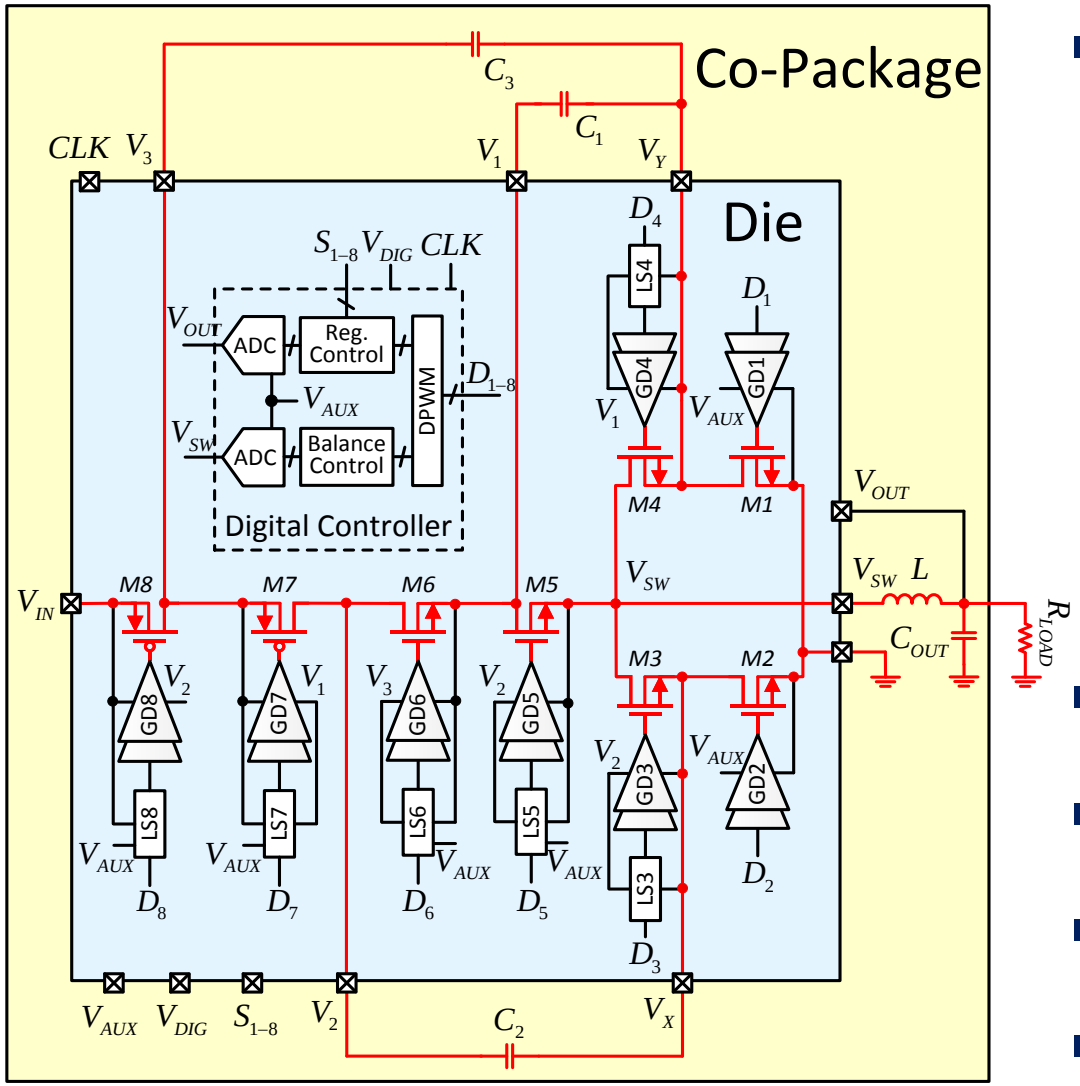
Hybrid SC Converter





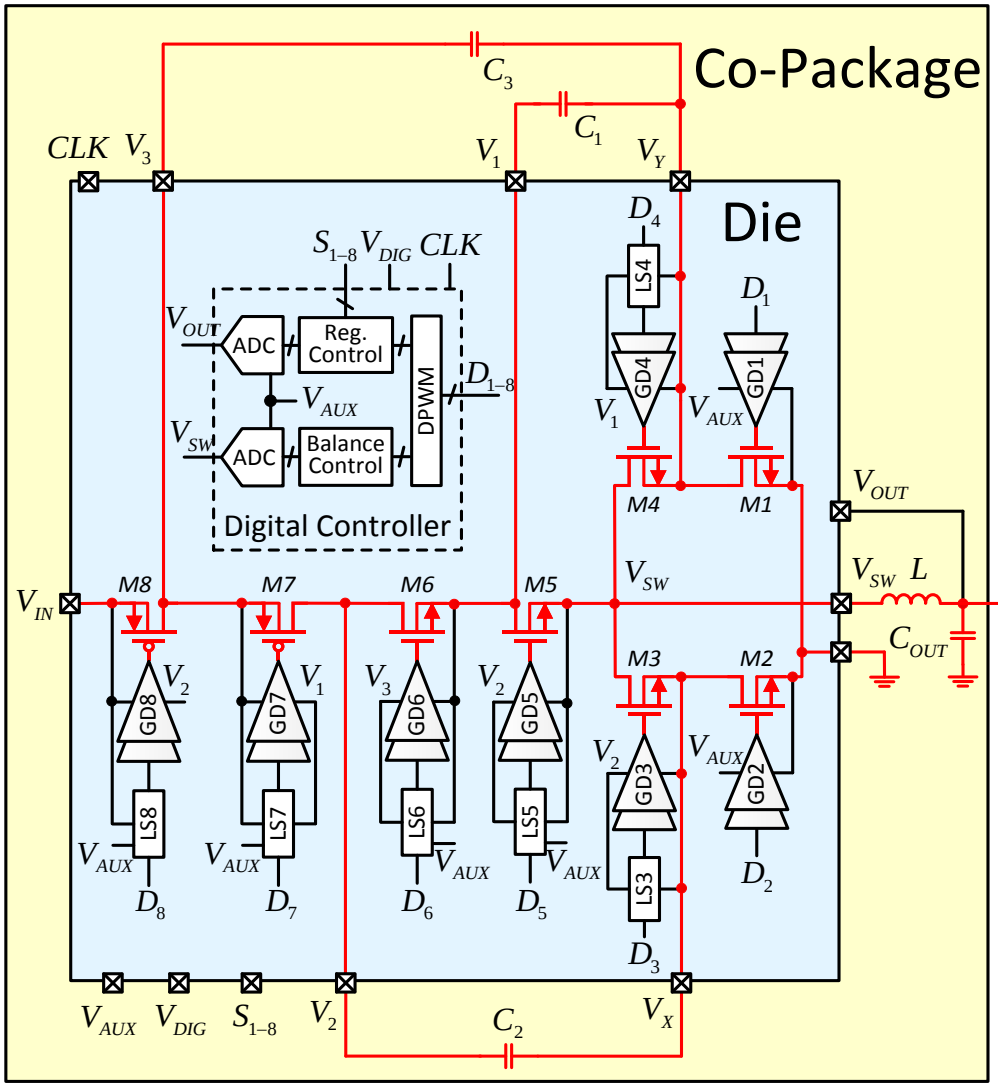
Y. Lei, R. May and R.C.N. Pilawa-Podgurski, “Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 770-782, Jan. 2016.

System Architecture



- Hybrid 4-to-1 Dickson converter
  - 8 power MOSFETs
  - 3 flying capacitors
  - 1 output capacitor
  - 1 inductor
- Gate driver (GD)
- Level shifter (LS)
- V_{out} regulation
- Cap. balancing

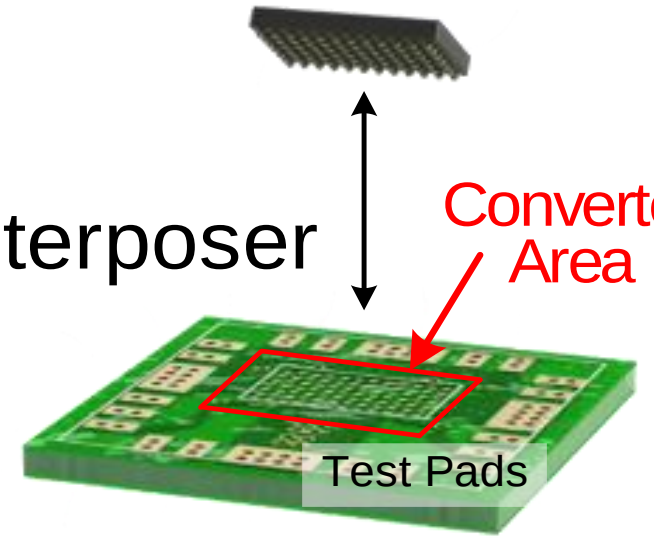
Package – High Current Density



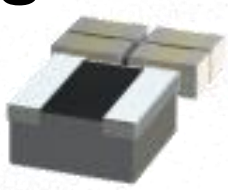
Die (Flipchip)

Interposer

Converter Area

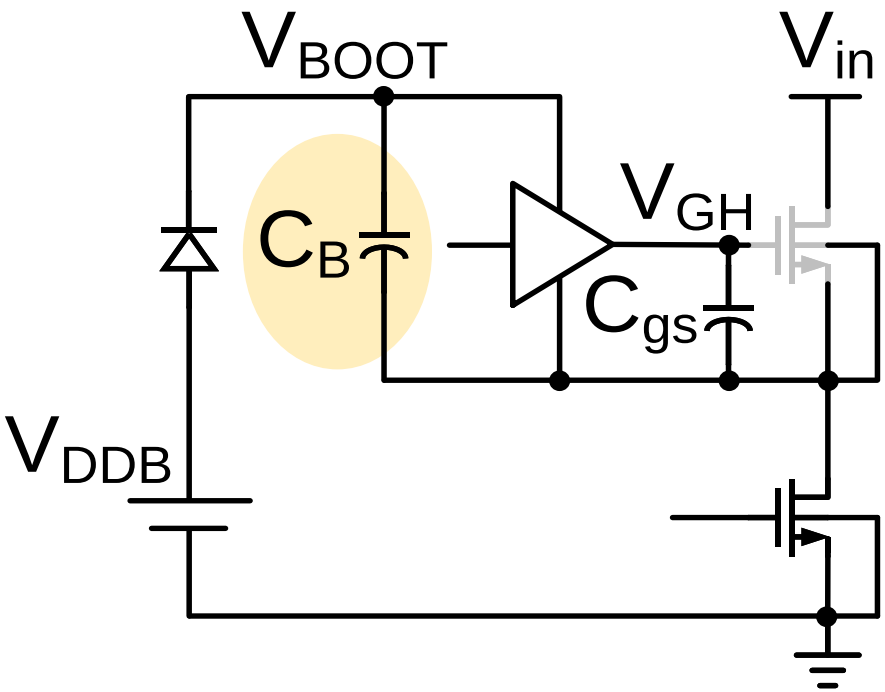


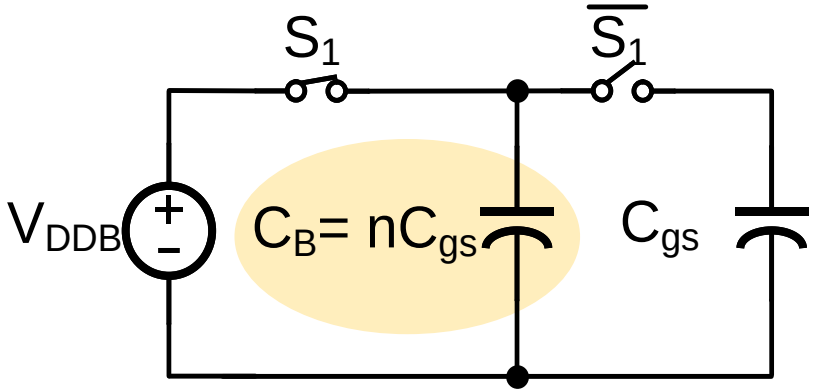
Passives



Capacitor Area Reduction

- Conventional boot-strap GD consumes considerable on-die C_B, e.g. $C_B = 10C_{gs}$
- Low V_{gs} increases $R_{ds,on}$ per area

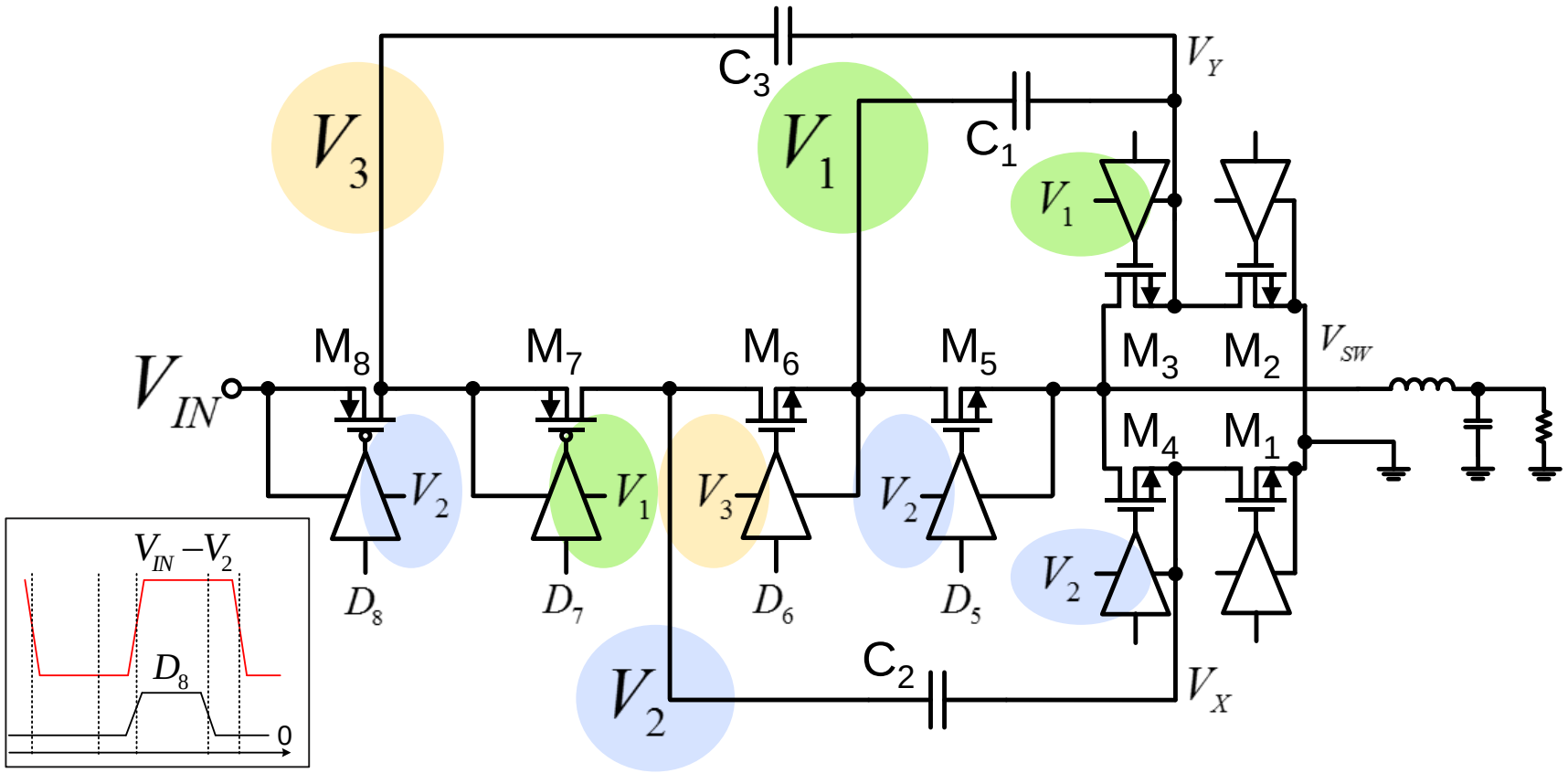




$$\frac{V_{gs}}{V_{DDB}} = 1 - \left(\frac{1}{n+1} \right)$$

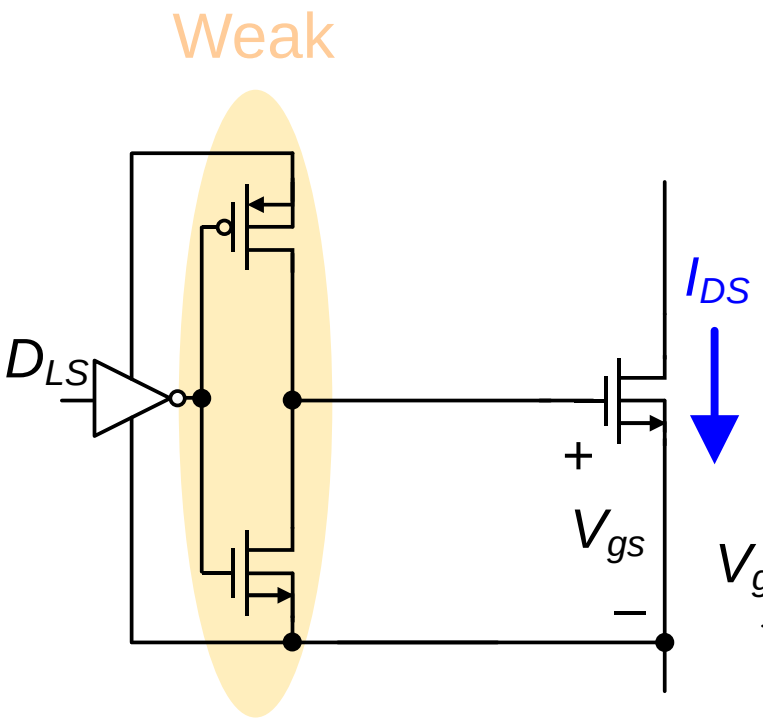
Voltage Borrowing Technique

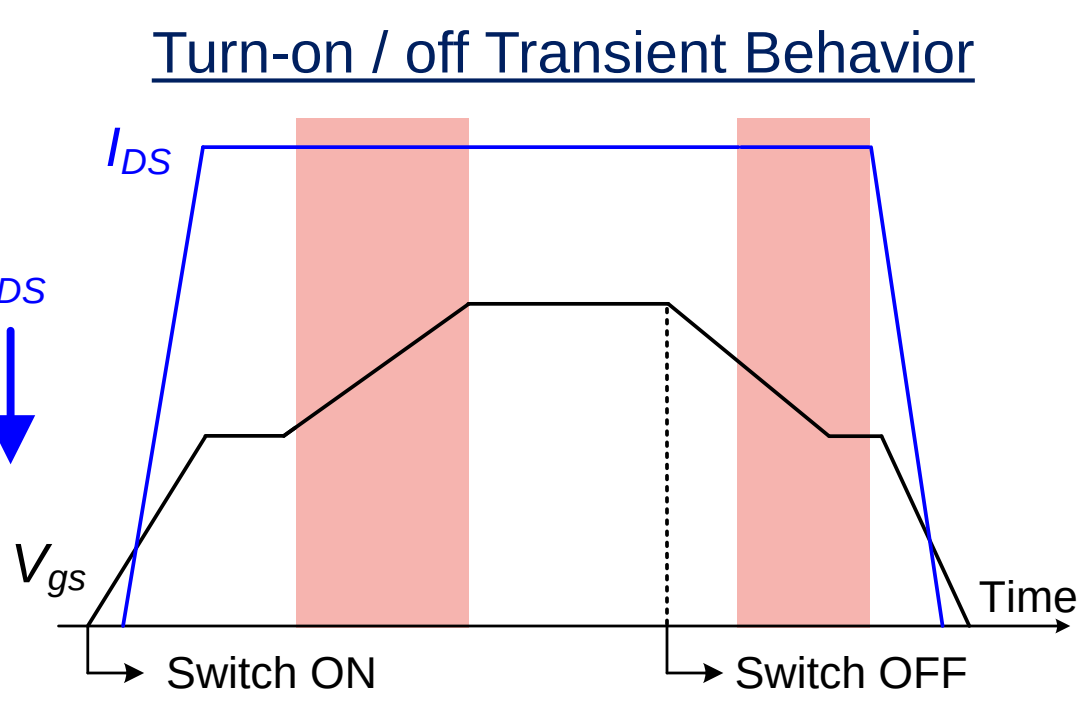
- Powered by existing flying capacitors
  - No extra capacitor needed
  - No extra voltage supply circuit needed



Ringing Reduction

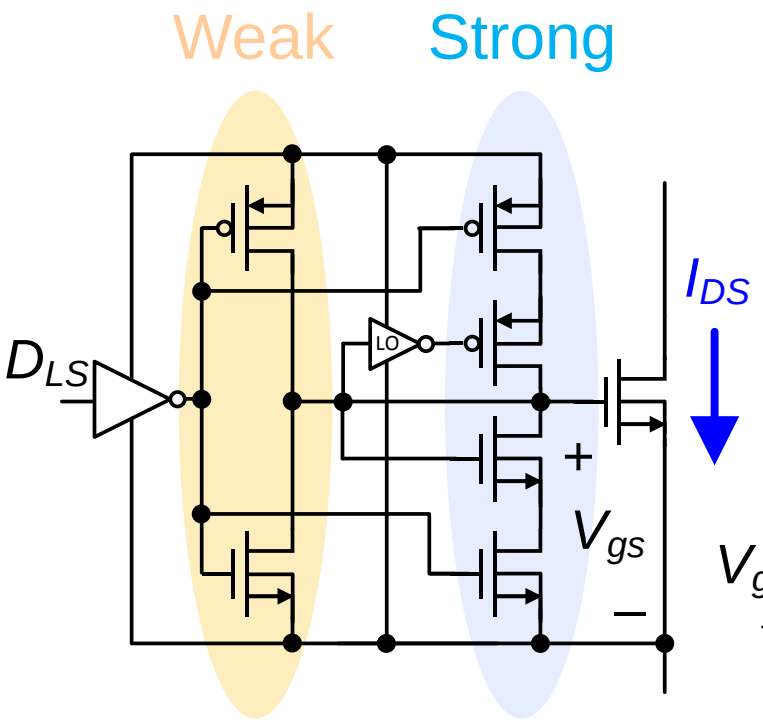
- Too fast transition: large ringing
- Too slow transition: low efficiency
  - Low V_{gs} increases conduction loss
  - Worse if running at higher switching frequency

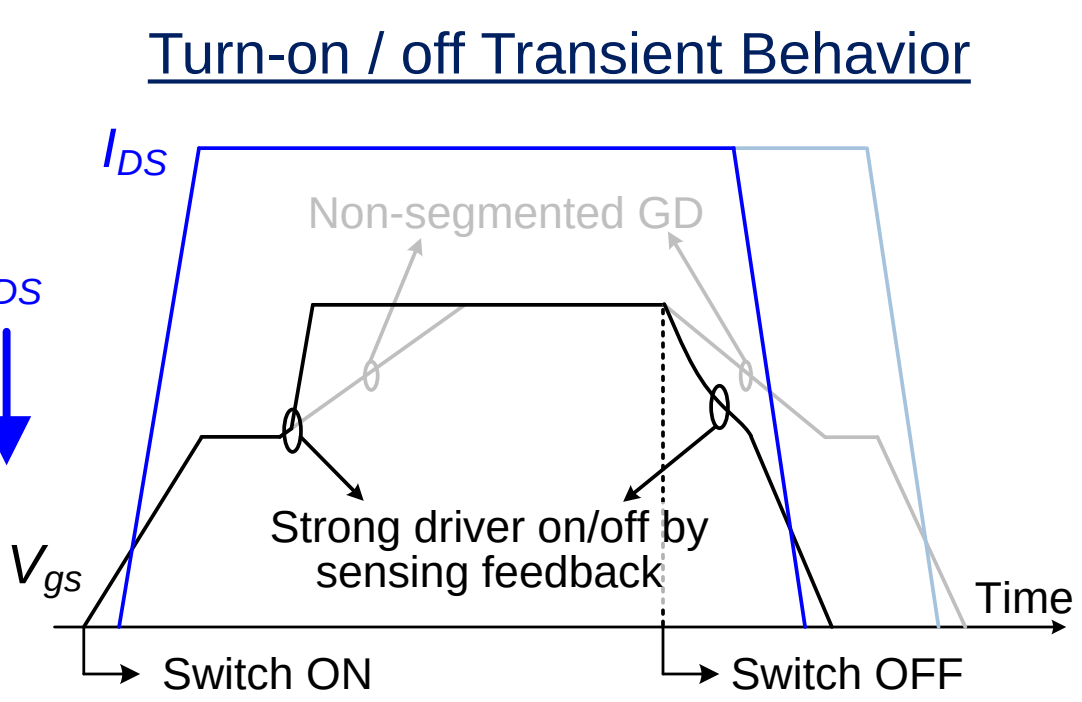




Segmented Gate Driver

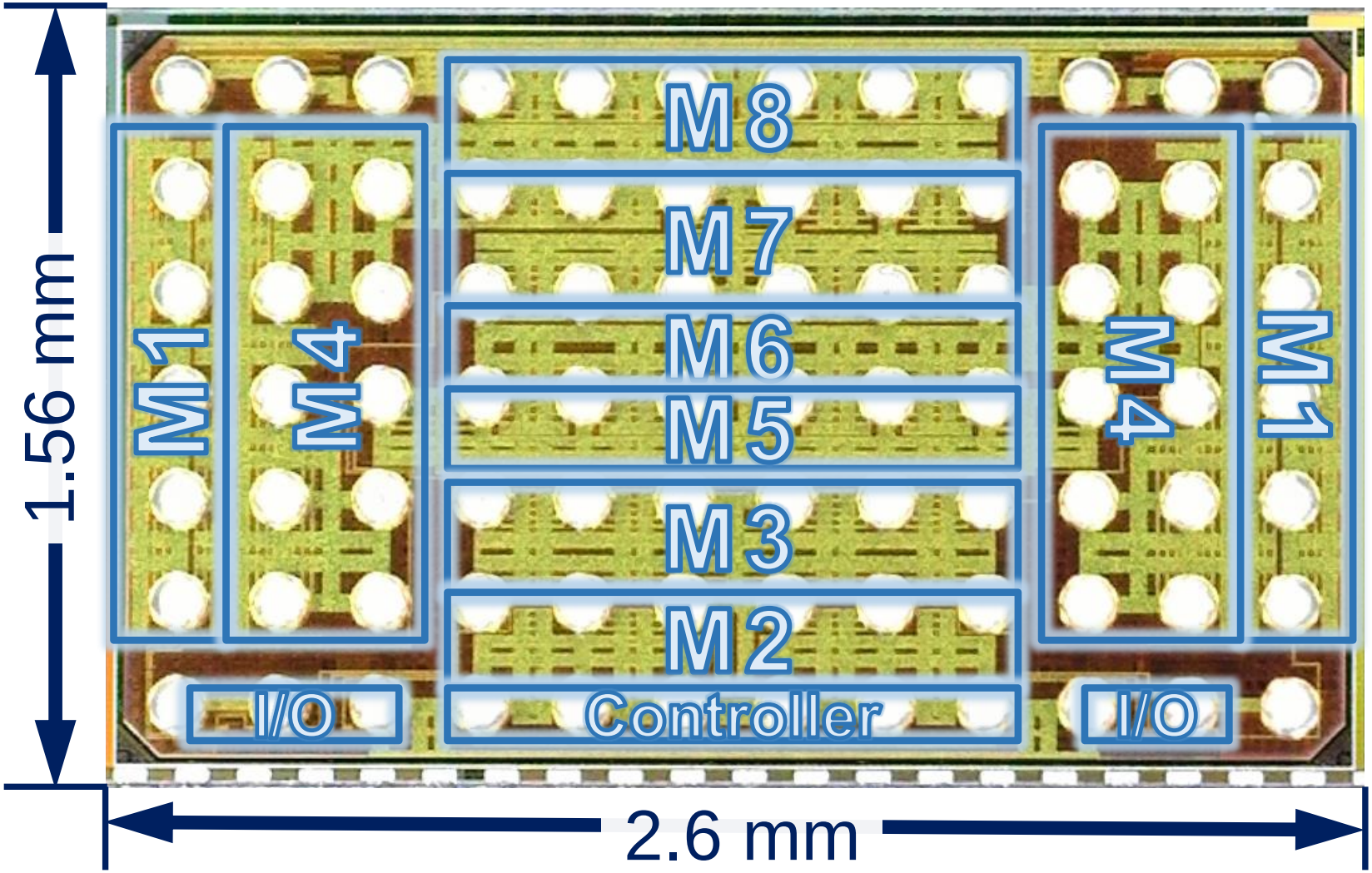
- Ringing reduction w/o sacrifice of efficiency
  - Weak driver first slows down the transition
  - Strong driver then raises V_{GS} at a faster rate so that the switch reaches the low $R_{ds,on}$ sooner





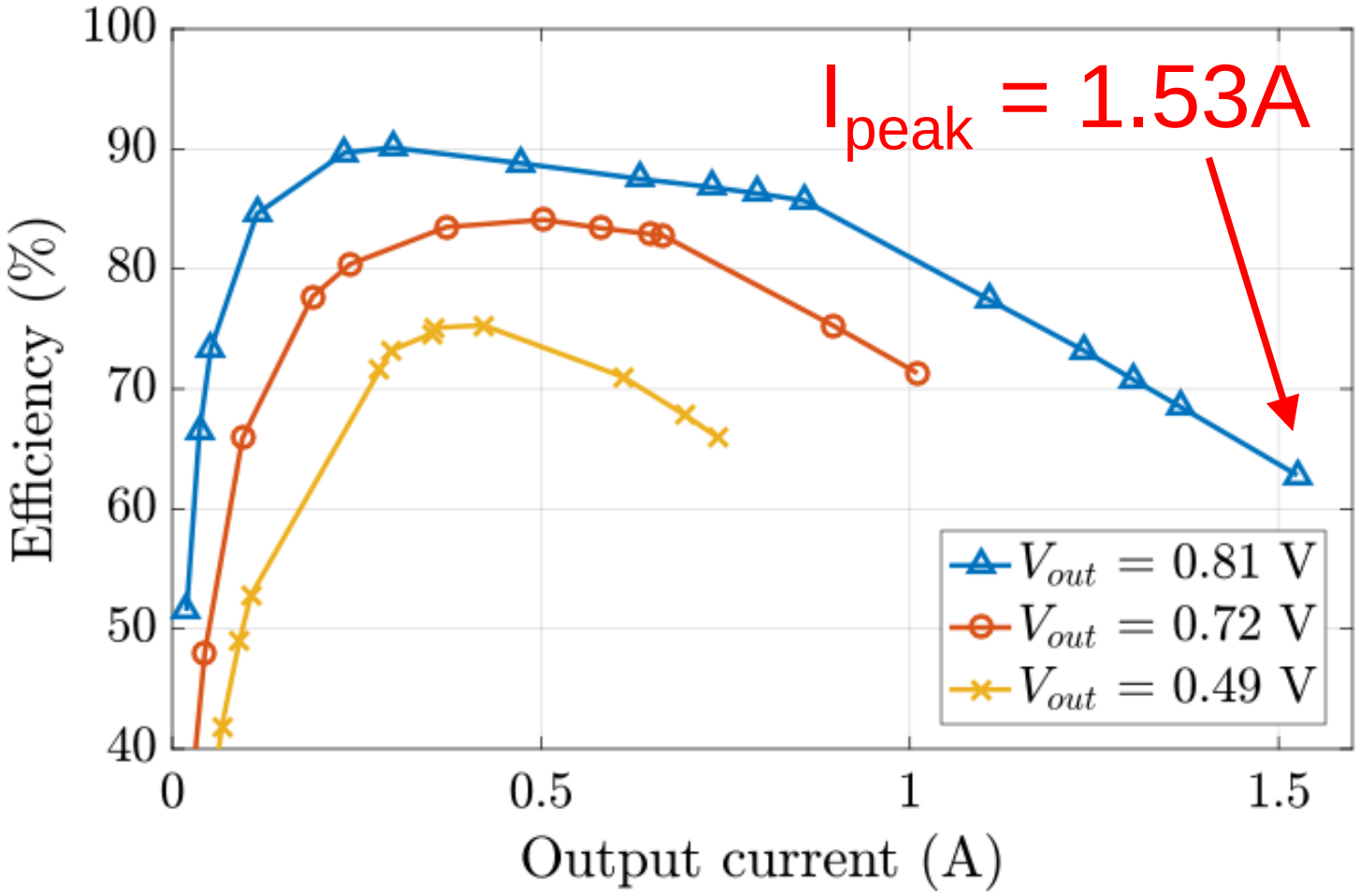
Die Micrograph

- 65nm bulk CMOS process



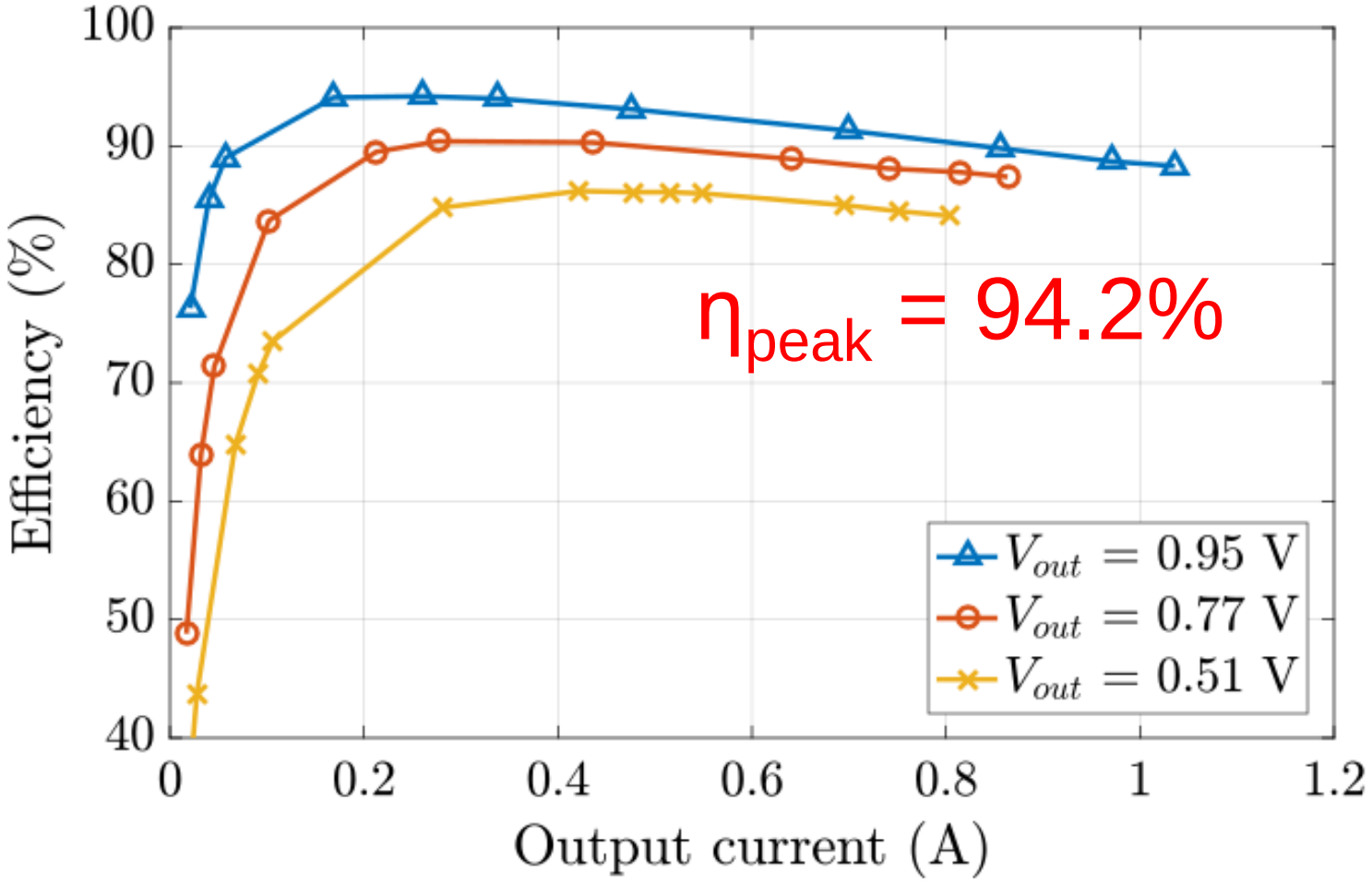
Measured Efficiency

- V_{in} = 4.2 V, L = 180 nH, DCR = 24 mΩ

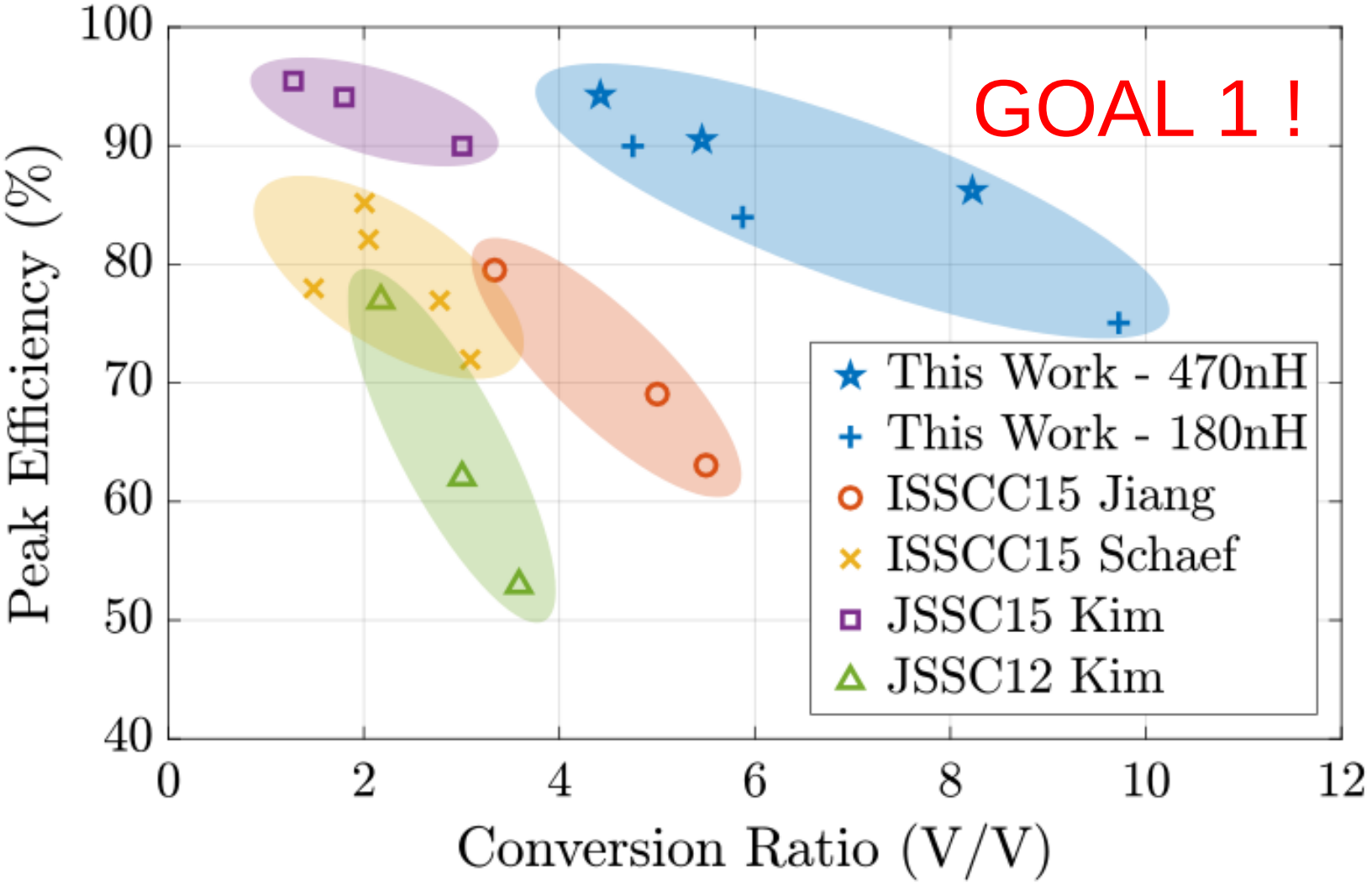


Measured Efficiency

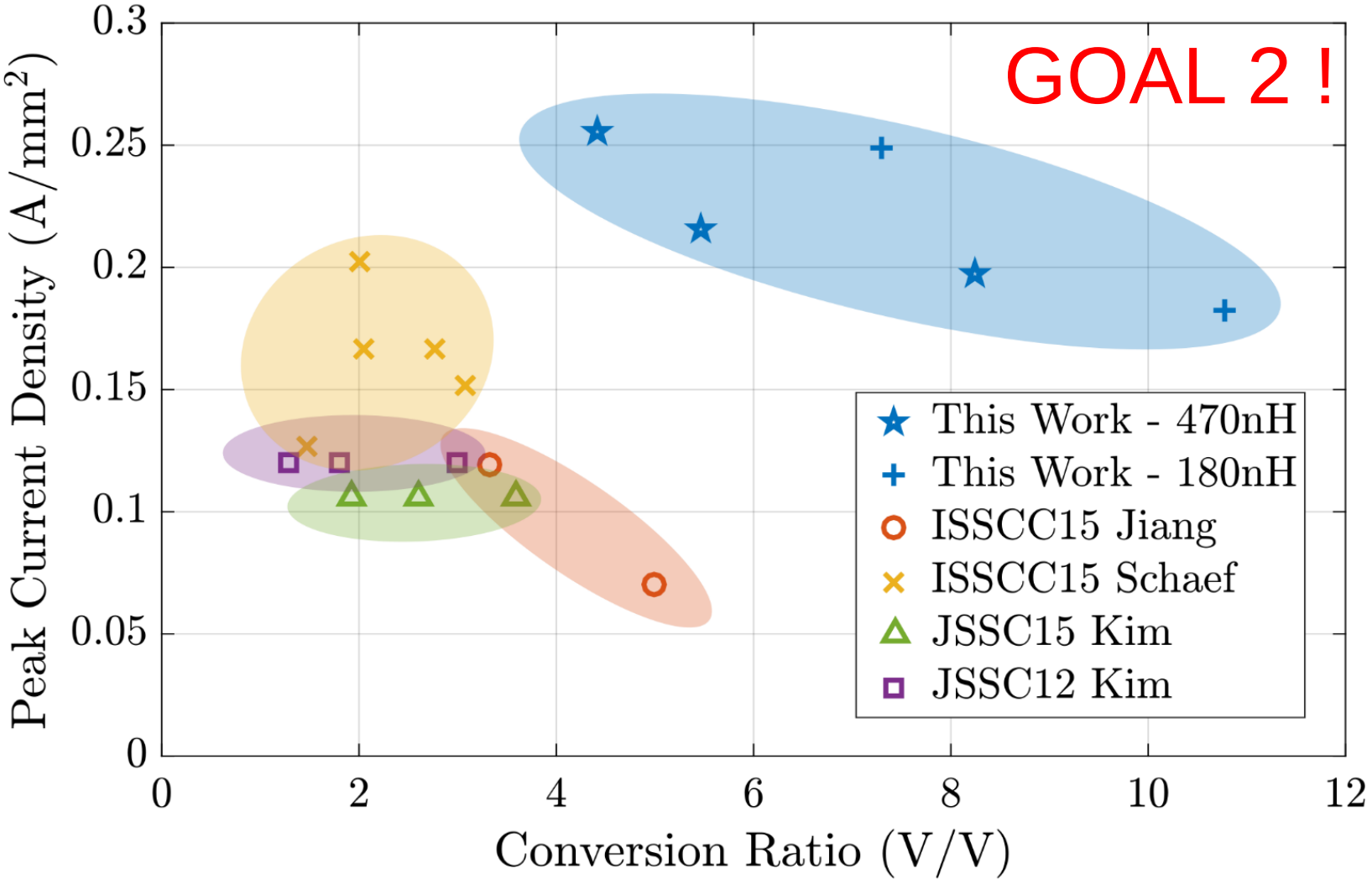
- V_{in} = 4.2 V, L = 470 nH, DCR = 8 mΩ



Performance Comparison



Performance Comparison



Conclusion

- First CMOS implementation of a hybrid Dickson SC converter
  - High power density and efficiency for high step-down
  - Good for low-voltage loads powered by Li-ion batteries
- Capacitor area reduction
  - Floating gate driver and level shifter are powered by the flying capacitors themselves
- Ringing reduction w/o sacrifice of efficiency
  - Segmented gate driver uses both slow and fast drivers

Acknowledgements

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Questions ?

Voltage Borrowing Technique

- Selected voltage
  - High enough to turn on switches with low $R_{ds,on}$
  - Within switch voltage ratings