A GaN-based Flying-Capacitor Multilevel Boost Converter for High Step-up Conversion

Zitao Liao, Yutian Lei and Robert C.N. Pilawa-Podgurski

University of Illinois Urbana-Champaign

Presented by Zitao Liao
Outline

- Motivation
- Hardware Design
- Experiment Results
- Conclusion
Motivation – Compact High Voltage DC Generation

- **Applications**
  - Satellite Propulsion System
    - Ion Thruster Unit
  - Pulse Electric Field (PEF)
    - Food and beverage preservation

- **Research Goals**
  - 100’s V to 1 kV Output, 1 kW power converter
    - 100 V and 200 V input voltage
  - High power density
  - High efficiency
Motivation

- Transformer Based Converters for HVDC generation
- High turn-ratio transformer
  - Bulky and costly
  - High rating devices on the high voltage side
Hardware Design - FCML Boost Converter

- Flying capacitor multilevel (FCML) converter
Hardware Design - FCML Boost Converter

- 7-level flying capacitor multilevel converter

- Phase-shifted PWM (PSPWM)
  - 6 PWM signals with phase shift of $360°/(N - 1) = 60°$
  - Same duty ratio as regular boost converter ($D = 0.9$ for 10x boost)

- Switching Node:
  - Period: $T_{fcml}/(N - 1)$
  - Ripple Amplitude: $V_{out}/(N - 1)$
- 7-level flying capacitor multilevel converter

- Natural balancing of flying capacitors
- S1 open: $V_{sw} = V_{c1} = \frac{1}{6}V_{out}$
- S2 open: $V_{sw} = V_{c2} - V_{c1} = \frac{2}{6}V_{out} - \frac{1}{6}V_{out}$
- **7-level flying capacitor multilevel converter**

- **Inductor size**

  \[ L_{f_{cml}} = \frac{(1-(1-D)(N-1))V_{in}}{\Delta I_L f_{sw}(N-1)} \]

  - Conventional boost converter is a 2-level (N=2) FCMC
  - With the same \( V_{in} \), \( D \), \( \Delta I_L \), and \( f_{sw} \), \( L_{f_{cml}} \) is 13.5 times smaller when \( N=7 \) than when \( N=2 \).

- **Switch Rating**: \( \frac{V_{out}}{N-1} \)
  - 200 V GaN Switch
  - Fast switching transition
  - low \( R_{ds\_on} \)
Hardware Design - Switching Cell

- **Gate driving**
  - ADUM5210 isolated DC-DC for level shifting
  - LM5114 low-side driver

- **Switching cell PCB**
  - EPC2034 GaN switches and low-side drivers
  - Diodes

- **Local decoupling capacitors**
  - Reduce ringing caused by parasitics
## Hardware Design - FCML Boost Converter

<table>
<thead>
<tr>
<th>Measurement</th>
<th>Dimension (L x W X H)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectangular box of the PCB</td>
<td>3.8 in x 2.2 in x 0.54 in</td>
</tr>
<tr>
<td>Rectangular box of the Power Stage</td>
<td>3.6 in x 0.67 in x 0.54 in</td>
</tr>
</tbody>
</table>
Hardware Design - Flying capacitors

- Ceramic Capacitor
  - High energy density, low ESR and ESL
  - Capacitance decreases with increasing voltage bias

- 1 kV rated flying capacitor implementation
  - 1 kV rated capacitors in parallel or lower rating capacitors in series

- 0.47 µF, 1 kV capacitor, Knowles Syfers
  - Degrade to 50nF @ 1 kV
  - Energy density @ 1 kV is 0.183 mJ/mm\(^3\)

- 2.2 µF, 450 V capacitor, TDK
  - Degrade to 0.55 µF @ 1 kV
  - Energy density @ 1 kV is 0.78 mJ/mm\(^3\)
Hardware Design- Flying capacitors

- 2.2 µF, 450 V capacitor x6
- Voltage Balancing Resistors
  - $Q = C_1 V_1 = C_2 V_2$
  - $V_1 >> V_2$, exceeding rated voltage
- 200 V, 2 A
- Low Reverse Recovery Charge
  - High voltage (>100 V) Schottky still have significant reverse recovery current because of guard-ring p-n junction diode

S320 Schottky diode reverse recovery current (2 V to 20 V conversion, 1 A input current).
## Selected tested diodes

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Parameters</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fairchild S320</td>
<td>200 V, 3 A</td>
<td>General Purpose Schottky</td>
</tr>
<tr>
<td>PDS3200</td>
<td>200 V, 3 A</td>
<td>General Purpose Schottky</td>
</tr>
<tr>
<td>STMicro STPS2200</td>
<td>200 V, 2 A</td>
<td>Power Schottky</td>
</tr>
<tr>
<td>SBR10U</td>
<td>200 V, 10 A</td>
<td>Super Barrier</td>
</tr>
<tr>
<td>VS2EFH02</td>
<td>200 V, 3 A</td>
<td>Hyperfast Reverse Recovery</td>
</tr>
</tbody>
</table>

### Graph

- **X-axis**: Input Power (W)
- **Y-axis**: Power Losses (W)

- **Diodes**: S320, PDS3200, STPS2200, SBR10U, VS2EFH02

---

### Table

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Parameters</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fairchild S320</td>
<td>200 V, 3 A</td>
<td>General Purpose Schottky</td>
</tr>
<tr>
<td>PDS3200</td>
<td>200 V, 3 A</td>
<td>General Purpose Schottky</td>
</tr>
<tr>
<td>STMicro STPS2200</td>
<td>200 V, 2 A</td>
<td>Power Schottky</td>
</tr>
<tr>
<td>SBR10U</td>
<td>200 V, 10 A</td>
<td>Super Barrier</td>
</tr>
<tr>
<td>VS2EFH02</td>
<td>200 V, 3 A</td>
<td>Hyperfast Reverse Recovery</td>
</tr>
</tbody>
</table>
Experiment Results

- High voltage test setup
Flying capacitor voltage balancing

Measured flying capacitor voltages during a input voltage transient from 0 V to 10 V, 20 W output power, 100 V output
Experiment Results

- **Switching node voltage**
  - Maximum voltage:

  Natural Balancing Voltage + Capacitor voltage ripple + Capacitor voltage increments

  (load current) (unbalanced charging/discharging cycle)

Switching node voltage ($V_{in} = 100 \text{ V}, V_{out} = 914 \text{ V}, P_{out} = 750 \text{ W}$)
Efficiency Measurements

- 1 kV output voltage
## Final Performance

<table>
<thead>
<tr>
<th></th>
<th>D = 0.9</th>
<th>D = 0.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum output power</td>
<td>750 W</td>
<td>900 W</td>
</tr>
<tr>
<td>Peak efficiency (power stage)</td>
<td>92.7% @700 W input power</td>
<td>93.7% @ 836.4 W input power</td>
</tr>
<tr>
<td>MCU power</td>
<td></td>
<td>1.4 W</td>
</tr>
<tr>
<td>Gate driving power</td>
<td>0.64 W</td>
<td></td>
</tr>
<tr>
<td>Power stage power density</td>
<td>660.2 W/in³</td>
<td>792.2 W/in³</td>
</tr>
<tr>
<td>Overall power density</td>
<td>166 W/in³</td>
<td>199.2 W/in³</td>
</tr>
</tbody>
</table>
Experiment Results

- **Loss Breakdown**
  - Loss breakdown at 750 W output power for 100 V to 916 V conversion
  
- **The largest portion of loss is from the extra switching loss introduced by reverse recovery current**
Conclusion

- FCML converter for high step-up conversion at kV and kW level
  - High power density and efficiency
- High voltage ceramic capacitor implementation

Future work
- More optimization to minimize reverse recovery loss
- Simpler level shifting circuits
- Control analysis
- Natural balancing analysis