DIGITAL INTERLEAVED PWM FOR ENVELOPE TRACKING CONVERTERS

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ABSTRACT

The bandwidth of a switched power converter is limited by Nyquist sampling theory. Further, switching frequency and the filtering structures of the converter are further limited to maintain high efficiency, low cost and size. A solution around this is to interleave power stages. Interleaving with analog PWM is well understood and used widely. This presentation will focus on digital PWM interleaving which makes it possible to get large usable bandwidth at relatively low switching frequencies. The mapping of the input signal to the different interleaved stages varies with the level of the signal and is nontrivial. Interleaving scheme with two, three and four switches will be demonstrated. Digital PWM created by counting a high speed clock has quantized duty ratios. The integral of these quantization errors can add up to large offsets in the currents in the interleaved stages. A scheme is introduced to eliminate current offsets without any feedback from the power stage. Simulation results will be shown for a dual interleaved system tracking single tone signals and an LTE-20 envelope. Higher order interleaving can provide even greater tracking bandwidth at lower switching frequencies.
Envelope Tracking System

RF Amplifier with Envelope Tracking Modulator
Envelope Bandwidth, Peak to Average Ratio and Spectral Efficiency

<table>
<thead>
<tr>
<th>Standard</th>
<th>Launched</th>
<th>Typ. Carrier BW (MHz)</th>
<th>Typ. Spectral Efficiency (bps/Hz)</th>
<th>Approx. PAPR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2G cellular</td>
<td>GSM</td>
<td>1991</td>
<td>0.2</td>
<td>0.17</td>
</tr>
<tr>
<td>Digital TV</td>
<td>DVB-H</td>
<td>2007</td>
<td>8</td>
<td>0.28</td>
</tr>
<tr>
<td>2.75G cellular</td>
<td>GSM + EDGE</td>
<td>2003</td>
<td>0.2</td>
<td>0.33</td>
</tr>
<tr>
<td>3G cellular</td>
<td>WCDMA FDD</td>
<td>2001</td>
<td>5</td>
<td>0.51</td>
</tr>
<tr>
<td>Digital TV</td>
<td>DVB-T</td>
<td>1997</td>
<td>8</td>
<td>0.55</td>
</tr>
<tr>
<td>Wi-Fi</td>
<td>IEEE 802.11a/g</td>
<td>2003</td>
<td>20</td>
<td>0.90</td>
</tr>
<tr>
<td>WiMAX</td>
<td>IEEE 802.16d</td>
<td>2004</td>
<td>20</td>
<td>1.20</td>
</tr>
<tr>
<td>Wi-Fi</td>
<td>IEEE 802.11n</td>
<td>2007</td>
<td>20</td>
<td>2.40</td>
</tr>
<tr>
<td>3.5G cellular</td>
<td>HSDPA</td>
<td>2007</td>
<td>5</td>
<td>2.88</td>
</tr>
<tr>
<td>3.9G cellular</td>
<td>LTE</td>
<td>2009</td>
<td>20</td>
<td>8.00</td>
</tr>
</tbody>
</table>
POWER SAVED BY ENVELOPE TRACKING

Constant supply

Variable envelope

Energy dissipated as heat
OBJECTIVES OF DIGITAL INTERLEAVED ENVELOPE TRACKER

- High efficiency, high bandwidth switcher with digital input to produce with high fidelity output voltage to drive a dynamic load
- Switching frequency kept relatively low (10’s of MHz) to keep efficiency high while maintaining very high bandwidth (10’s of MHz)
- Conversion directly from digital reference to digital PWM in the digital domain
- Extremely high current slew rate (~100A/µs)
- Current is shared between interleaved stages
- Switching frequency and its odd harmonics are cancelled
- High linearity and low noise
Signal Flow Diagram for N Stage Interleaving

FIG. 1
SAMPLE RATE WITH DIGITAL INTERLEAVING

- Each PWM edge of each stage is an independent sample
- There are two PWM edges (rising and falling) per PWM period
- Sample rate with N stages = 2.N.Fsw
  - 4Fsw with dual stage
  - 6Fsw with triple stage
  - 8.Fsw with quad stage
OVERALL SYSTEM FOR 2 STAGE INTERLEAVING

FIG. 2
OVERALL SYSTEM FOR 3 STAGE INTERLEAVING

FIG. 3
OVERALL SYSTEM FOR 4 STAGE INTERLEAVING
Signal Flow Diagram for 2 Stage Interleaving

Block Diagrams of PCM to Dual Digital PWM for Envelope Tracking

**FIG. 5**
Signal Flow Diagram for 3 Stage Interleaving
SIGNAL FLOW DIAGRAM FOR 4 STAGE INTERLEAVING

BLOCK DIAGRAMS OF PCM TO QUAD DIGITAL PWM FOR ENVELOPE TRACKING

NOISE SHAPER 702 → DUTY RATIO QUANTIZER 704 → SINGLE TO QUAD MAPPING UNIT 706 → IMBALANCE CORRECTION 708 → QUAD COUNTER 714

DUTY RATIO AT 8Fsw

CORRECTED PCM AT 8Fsw 703

PCM AT 8Fsw 401

DUTY RATIO AT 8Fsw 705

QUANTIZED IMBALANCE ERROR4 731

QUANTIZED IMBALANCE ERROR3 729

QUANTIZED IMBALANCE ERROR2 727

QUANTIZED IMBALANCE ERROR1 725

D1 AT 2Fsw 707

D2 AT 2Fsw 709

D3 AT 2Fsw 711

D4 AT 2Fsw 713

DC1 AT 2Fsw 715

DC2 AT 2Fsw 717

DC3 AT 2Fsw 719

DC4 AT 2Fsw 721

PWM2 AT Fsw 405

PWM1 AT Fsw 403

PWM4 AT Fsw 409

PWM3 AT Fsw 407

IMBALANCE ERROR 723

IMBALANCE ERROR ACCUMULATOR 710

FIG. 7
STATE DIAGRAM FOR TWO STAGE INTERLEAVING

\[ \frac{1}{2} < PCM < 1 \]

\[ PCM < \frac{1}{2} \]

FIG. 8
MAPPING OF PCM INPUT TO PWM DUTY RATIOS FOR TWO STAGE INTERLEAVING

FIG. 9
### Duty Ratios, Transition Times and States for Dual Stage Interleaving

#### Table 1 Dual PWM Truth Table

<table>
<thead>
<tr>
<th>Q</th>
<th>PCM value</th>
<th>PWM$_1$ at start</th>
<th>PWM$_2$ at start</th>
<th>Start state</th>
<th>PWM$_1$ at end</th>
<th>PWM$_2$ at end</th>
<th>End state</th>
<th>Signal change</th>
<th>Signal Change time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q$_1$</td>
<td>&lt;0.5</td>
<td>1</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>A</td>
<td>PWM$_1$</td>
<td>(2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td></td>
<td>&gt;0.5</td>
<td>1</td>
<td>0</td>
<td>C</td>
<td>1</td>
<td>1</td>
<td>D</td>
<td>PWM$_2$</td>
<td>(2-2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td>Q$_2$</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>A</td>
<td>0</td>
<td>1</td>
<td>B</td>
<td>PWM$_2$</td>
<td>(1-2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>D</td>
<td>0</td>
<td>1</td>
<td>B</td>
<td>PWM$_1$</td>
<td>(2pcm-1)T$_{sw}$/4</td>
</tr>
<tr>
<td>Q$_3$</td>
<td>&lt;0.5</td>
<td>0</td>
<td>1</td>
<td>B</td>
<td>0</td>
<td>0</td>
<td>A</td>
<td>PWM$_2$</td>
<td>(2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td></td>
<td>&gt;0.5</td>
<td>0</td>
<td>1</td>
<td>B</td>
<td>1</td>
<td>1</td>
<td>D</td>
<td>PWM$_1$</td>
<td>(2-2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td>Q$_4$</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>A</td>
<td>1</td>
<td>0</td>
<td>C</td>
<td>PWM$_1$</td>
<td>(1-2pcm)T$_{sw}$/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>1</td>
<td>D</td>
<td>1</td>
<td>0</td>
<td>C</td>
<td>PWM$_2$</td>
<td>(2pcm-1)T$_{sw}$/4</td>
</tr>
</tbody>
</table>
STATE DIAGRAM FOR THREE STAGE INTERLEAVING

\[
\frac{2}{3} < \text{PCM} < 1 \\
\text{HEHGFHEHGFHEHGF}
\]

\[
\frac{1}{3} < \text{PCM} < \frac{2}{3} \\
\text{BECGDFBECGDFBECGDF}
\]

\[
0 < \text{PCM} < \frac{1}{3} \\
\text{BACADABACADABACADA}
\]
MODE PATTERNS FOR DIFFERENT SIGNAL LEVELS OF THREE STAGE INTERLEAVING

When $0 < \text{PCM} < \frac{1}{3}$ the transitions follow the pattern:
BACADABACADABACADA.

When $\frac{1}{3} < \text{PCM} < \frac{2}{3}$ the transitions follow the pattern:
BECGDFBECGDFBECGDF.

When $\frac{2}{3} < \text{PCM} < 1$ the transitions follow the pattern:
HEHGFHEHGHFHEHGHF.
SWITCHING WAVEFORMS FOR PCM < 1/3 FOR A THREE STAGE INTERLEAVING CONVERTER

FIG. 11
SWITCHING WAVEFORMS FOR $1/3 < \text{PCM} < 2/3$ FOR A THREE STAGE INTERLEAVING CONVERTER

FIG. 12

[Diagram showing PWM waveforms for PWM3, PWM2, and PWM1 with labels B, E, C, G, D, F]
SWITCHING WAVEFORMS FOR PCM > 2/3 FOR A THREE STAGE INTERLEAVING CONVERTER

FIG. 13
STATE DIAGRAM FOR FOUR STAGE INTERLEAVING

\[ \frac{3}{4} < PCM < 1 \]
\[ MPLPONPMPLPONPMPLPONP \]

\[ \frac{1}{2} < PCM < \frac{3}{4} \]
\[ MLHOKNIMLHOKNIMLHOKNI \]

\[ \frac{1}{4} < PCM < \frac{1}{2} \]
\[ BFCHDKEIBFCHDKEIBFCHDKEI \]

\[ 0 < PCM < \frac{1}{4} \]
\[ BACADAEABACADAEABACADAEA \]
MODE PATTERNS FOR DIFFERENT SIGNAL LEVELS OF FOUR STAGE INTERLEAVING

When 0<PCM<1/4 the transitions follow the pattern:
BACADAEABACADAEABACADAEA.

When 1/4<PCM<1/2 the transitions follow the pattern:
BFCHDKEIBFCHDKEIBFCHDKEI.

When 1/2<PCM<3/4 the transitions follow the pattern:
MFLHOKNIMFLHOKNIMFLHOKNI.

When 3/4<PCM<1 the transitions follow the pattern:
MPLPOPNPMPMLPOPNPMPMLPOPNP.
SWITCHING WAVEFORMS FOR PCM < 1/4 FOR A FOUR STAGE INTERLEAVING CONVERTER

FIG. 15
SWITCHING WAVEFORMS FOR 1/4 < PCM < 1/2
FOR A FOUR STAGE INTERLEAVING CONVERTER
SWITCHING WAVEFORMS FOR 1/2 < PCM < 3/4 FOR A FOUR STAGE INTERLEAVING CONVERTER
SWITCHING WAVEFORMS FOR PCM > 3/4 FOR A FOUR STAGE INTERLEAVING CONVERTER

FIG. 18
EXAMPLE POWER STAGE FOR DUAL INTERLEAVING CONVERTER

FIG. 19

- DC 109
- RA₂ 206
- RA₁ 204
- RB₂ 1904
- RB₁ 1902
- L₂ = 70 nH 214
- IL₂ 209
- L₁ = 70 nH 212
- IL₁ 207
- L₃ = 25 nH 1906
- V_CUT 113
- C₁ = 2.2 nF 1908
- C₂ = 0.53 nF 1910
IMBALANCE CORRECTION THEORY

- Quantization noise is a random number with a uniform distribution.
- The current in each inductor is determined by the integral of the individual switch voltage.
- Rather than measure the currents in the inductor with a current sensor and ADC, we estimate the current imbalance by integrating the quantization errors.
- Imbalance Correction Unit produces a step change in duty ratio when the accumulated error exceeds a certain level.
- The Imbalance Correction Unit also helps cancel the switching frequency at the output of the system.
- The system is entirely digital requiring no feedback from the power stage or any analog components.
- Under normal operation, the imbalance correction block does not modify any of the PWM signals.
Quantization Noise Adding up to Create Large Current Imbalance

Inductor Currents Without Imbalance Correction

FIG. 20
Quantization Noise Imbalance Corrected to Eliminate Current Imbalance

**Fig. 21**

*Inductor Currents with Imbalance Correction*
**Single Tone and LTE20 Simulations**

- Power stage with filter as shown in fig. 19
- Switching frequency is cancelled
- Twice the switching frequency is about 80dB lower than the desired signal
- Nonlinearity is at a level 70 to 80 dB below desired signal
- LTE-20 is a 4G signal using 20 MHz RF channel
- Bandwidth of I and Q are individually 10 MHz
- Lowpass filter passes signals out to 30 MHz
SWITCHER OUTPUT SPECTRUM WITH 1 MHZ TONE

SINGLE TONE LARGE SIGNAL SPECTRUM (1 MHz)

Power Spectral Density

FIG. 22
SWITCHER OUTPUT SPECTRUM WITH 9 MHZ TONE

SINGLE TONE LARGE SIGNAL SPECTRUM (9 MHz)

FIG. 23
Switcher Output Spectrum with 18 MHz Tone

Power Spectral Density

Magnitude (dB)

Frequency (MHz)

FIG. 24
LTE20 SIMULATION SHOWING GOOD TRACKING

![Tracking of LTE20 Envelope](image)

FIG. 25
SWITCHER OUTPUT SPECTRUM PRODUCING LTE20 ENVELOPE

Power Spectral Density

Magnitude (dB)

-120 -100 -80 -60 -40 -20

0 20 40 60 80 100 120

Frequency (MHz)

FIG.26
SUMMARY

- A digital interleaved converter with N stages supports a data rate of $2N \cdot F_{sw}$
- The digital interleaved converter is able to transition over different signal levels seamlessly while maintaining current sharing
- Current sharing is maintained without feedback of current from the power stage
- All the operations are entirely in the digital domain for efficient implementation at high switching frequencies
- This method has been successfully applied to tracking an LTE-20 envelope signal