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Design Document

Analog PWM Amplifier

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Abstract:

The analog pulse width modulation amplifier was designed as an integrated "blue box" approach to demonstrating the PWM process. With suitable component selection, the resulting PWM is of sufficiently high quality to demonstrate not only motor drive applications but also audio amplification. The design realizes the PWM discretely: a voltage controlled oscillator to generate the ramp, a comparator, dead-time logic, and a full H bridge to drive the load. To simplify the gate drive circuitry, each gate is driven directly from the input bus. In practice this limits the bus voltage to the maximum V_{gs} of the FET – about 20V; sufficient to drive a small 8Ω speaker. Test points are provided to allow investigation of every aspect of the PWM process including dead-time.

Document Revision History

Issue	Date	Comments
000	9/14/2004	Initial Release
001	10/26/2007	Correction regarding demo unit

Contents

1. Introduction

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1.1 Scope

The primary end use of the Analog PWM amplifier was for demonstration of a high quality PWM process. The majority of the PWM integrated circuits commercially available to not make many of the PWM process signals available to the user. Building the PWM process from discrete components allows all signals at all phases of the PWM process to be examined.

1.2 Definitions

Dead-time: The time during which no switches in the H-bridge are gated on. The switches turn off and on in a break before make configuration to prevent shorting out of the bus voltage.
H-Bridge: The output of the PWM process is a full H-bridge that connects the load to the bus in either a positive polarity of a negative polarity. Depending on the switch configuration, the voltage across the load becomes either $+V_{bus}$ or $-V_{bus}$.
PWM – Pulse Width Modulation

1.3 References

Schematics:	SK0002 Rev 3
PCB Layout:	PB0003 Rev C

2. Specification

Parameter	Min.	Max.
Supply voltage:	12V	20V
Analog input:	-2V	+2V
Switching frequency:	~10kHz	>300kHz
Dead-time	200nS nom.	
Low pass filer	Second order response, 37.5kHz cut-off	

3. Theory of Operation

Pulse width modulation, when used as the basis for an amplifier, is termed a "class D" or sometimes "class S" circuit. The principle is that the switch duty ratios can be made to follow any desired waveform, provided that switching is fast. The duty ratio signal can be recovered with a simple low-pass filter.

3.1 Power Supply

The amplifier receives DC power through the 4 pin header J2. Pins are labeled as appropriate (see schematic and PCB artwork). For general lab experimentation, the only externally required voltage for the PWM AMP is V_{CC} (and ground). Depending on the desired amplitude of the output, V_{CC} can be selected within the range of $\mathbf{12 < V_{CC} < 20}$. Voltages less than 12V will not be enough to power the ICs. Voltages above 20V will damage the FET driver ICs.

The PWM amplifier is designed both electrically and mechanically to interface with a small 12 V open frame power supply. A piece of sheet steel connected to frame ground may be needed as a Faraday shield between the PWM AMP and the power supply. Further, a solid ground connection between the PWM AMP circuit common and the power supply frame ground is needed to minimize noise.

Alternatively, any commonly available laboratory power supply can be substituted as the power supply for instructional purposes. Two series linear regulators provide regulated 12V and 5V for internal use within the amplifier circuit.

3.2 Analog Input

Analog input is supplied through the 3.5mm stereo headphone jack. Internally, the left and right channels are summed into a mono signal. The attenuator POT R6 is a 50K linear variable resistor that attenuates the applied input signal prior to the comparator. Note that there are no op-amps or other circuit to provide gain in the traditional sense.

The input is ac coupled into the comparator stage through C2. R5 sets the dc bias (offset) on the analog input and can be adjusted to compensate for any drift in the PWM amplifier to achieve a 50% output waveform for a 0V input. Turning R5 CW increases the DC bias.

3.3 Carrier and PWM Generation

The PWM Amplifier process implements discretely conventional sine-triangle PWM techniques. The triangle carrier function is generated by the LM566 VCO labeled U1 as seen on page 1 of the schematic. The frequency of the triangle carrier is set by C1 and R3. Turning R3 CW (clock wise) increases the frequency. R23 sets the peak to peak amplitude of the triangle function. Turning R23 CW increases the amplitude. General purpose comparator LM311 is used to create the PWM waveform by comparing the modulating function (analog input) with the carrier function (triangle waveform). The triangle carrier, modulating function, and resulting PWM are available via test points on the PCB.

3.4 Dead-Time Circuit and Gate Drive

The PWM waveform resulting from the comparator stage is passed into the dead-time circuit comprised of U3 and U4 as seen on page 2 of the schematic. The result is two gate drive signals and their complement. These four gate drive signals ensure that one set of switches completely turns off before another set turns on. This break before make feature ensures that both switches in one leg of the H bridge output stage are not both on, eliminating the possibility for shoot-through current and FET failure. The four gate signals are available on the orange test points TP4-TP7.

Soft-start circuitry (R15, C11, C22, C23) provides approximately a 2ms startup period to allow the power supply to stabilize before the bridge is allowed to run.

3.5 Output Bridge

The output is a typical “H bridge” with four FET switches connected in a geometry that resembles the letter H. Switches M1 and M4 operate as a one pair and M2 and M3 operate as the second pair. When M1 and M4 are “ON” and M2 and M3 are “OFF”, positive voltage is imposed across the load resulting in a current path in the positive direction. When M1 and M4 are “OFF” and M2 and M3 are “ON”, negative voltage is imposed across the load and the current reversed polarity and flows in the negative direction.. Thus the H bridge can supply both positive and negative output voltages from a single supply.

The PWM Amplifier can be configured for half bridge operation by populating only M1 and M3 and placing jumper JMP1.

The gate voltages are driven directly from the bus voltage by Micrel MIC4424 low impedance gate driver ICs. This arraignment simplifies the gate drive circuitry by eliminating the need for high-side referenced gate signals. However, it imposes the constraint that the maximum bus voltage cannot exceed the V_{gs} of the FET – typically about 20V.

3.6 Low Pass Output Filter

The output square wave from the bridge is low-pass filtered by L1, L2, C19, and C20. The frequency response has a –3dB point at about 37.5 kHz and is characteristic of a 2 pole second order filter. The calculated frequency response of the output filter is shown below. For carrier frequencies above 100 kHz, the low pass filter should yield adequate performance and low standby ripple current.

3.7 Demonstration Unit

In October 2007, the demonstration unit was reported as "bad." The demo unit is a PWM amplifier integrated with a power supply rated 12 V @ 0.8 A. This power supply is just barely enough to support a speaker load. The unit was reported as having a short, but in fact, there was an operational problem.

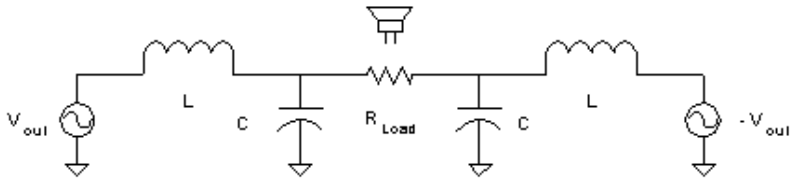
Basically, the power supply needs to stabilize before the amplifier starts switching. Otherwise, with a low-impedance load (e.g. 6 Ω), the power supply will go into current limit around 5 V and the rest of the circuitry will not work. Proper operation can be assured by simply waiting until the power supply is all the way active. The demo unit has a change to R15—now 100 kΩ to provide 200 ms delay.

Without this delay, the following scenarios were tested:

- Small power supply, 16 Ω load—good
- Bench power supply, 6 Ω load—good
- Small power supply, 6 Ω load—output constant at 5 V, with occasional blips

If the last scenario recurs, investigate more delay or a stronger power supply.

Output Filter for Analog PWM AMP



$L := 20 \times 10^{-6}$ $C := 900 \cdot 10^{-9}$

$R_{Load} := 8$

$$f_{-3db} = \frac{\frac{1}{\sqrt{L \cdot C}}}{2\pi} = 3.751 \times 10^{4}$$

$$\frac{\frac{R_{Load}}{L}}{2\pi} = 6.366 \times 10^{4}$$

Full Bridge: KCL & KVL Equations

$$\frac{V_i - V_1}{j \cdot w \cdot L} = \frac{V_1}{\frac{1}{j \cdot w \cdot C}} + \frac{V_1 - V_2}{R_{Load}} \quad (1)$$

$$\frac{V_1 - V_2}{R_{Load}} = \frac{V_2}{\frac{1}{j \cdot w \cdot C}} + \frac{V_2 - (-V_i)}{j \cdot w \cdot L} \quad (2)$$

$$V_{out} = V_1 - V_2 \quad (3)$$

Substitute (3)

$$\frac{V_i - V_1}{j \cdot w \cdot L} = \frac{V_1}{\frac{1}{j \cdot w \cdot C}} + \frac{V_{out}}{R_{Load}}$$

Substitute (3)

$$\frac{V_{out}}{R_{Load}} = \frac{V_2}{\frac{1}{j \cdot w \cdot C}} + \frac{V_2 - (-V_i)}{j \cdot w \cdot L}$$

Solve for V_2

$$V_2 = -V_{out} + V_1$$

$$\frac{V_{out}}{V_i} = \frac{-2}{L \cdot C \cdot w^2 - \frac{2 \cdot i \cdot w \cdot L}{R_{Load}} - 1}$$

$$V_1 = -i \cdot \frac{\left(V_{out} \cdot w \cdot L + i \cdot w^2 \cdot C \cdot R_{Load} \cdot L \cdot V_{out} - i \cdot R_{Load} \cdot V_{out} + i \cdot R_{Load} \cdot V_i\right)}{R_{Load} \cdot \left(w^2 \cdot C \cdot L - 1\right)}$$

$$A(w) := 20 \cdot \log\left[\left|\frac{2}{1 + (j w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right|\right]$$

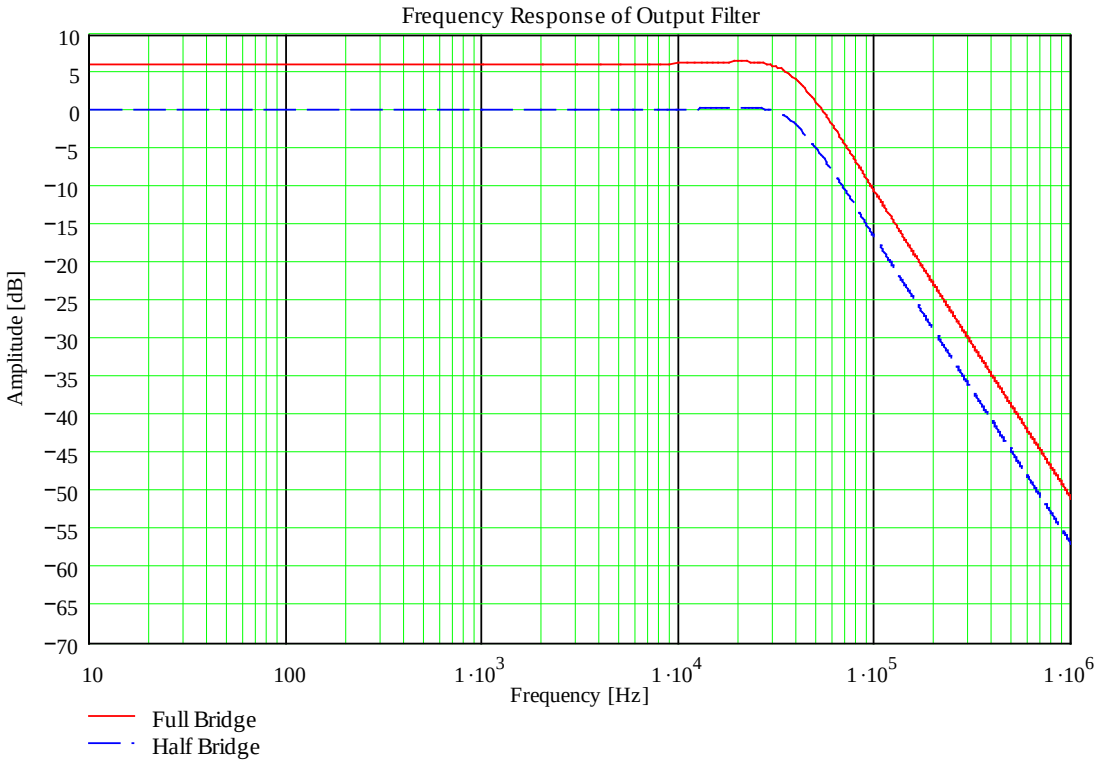
Half Ckt transfer function

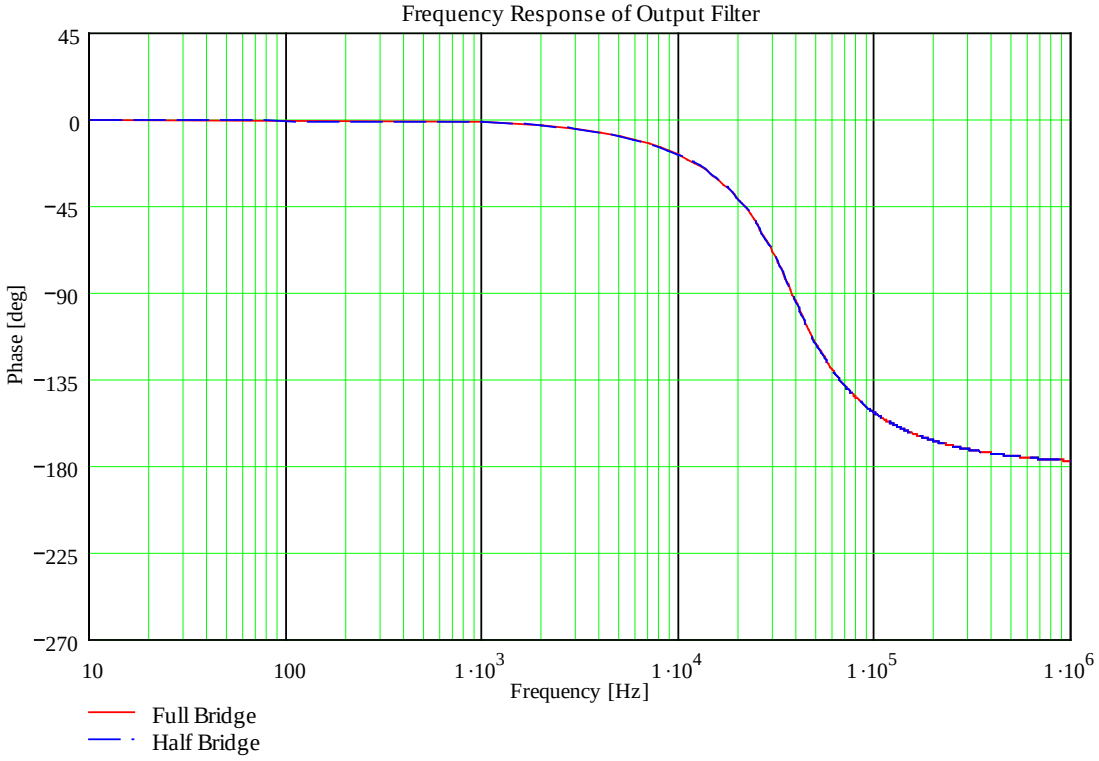
$$H(w) := 20 \cdot \log\left[\left|\frac{1}{1 + (j \cdot w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right|\right]$$

$$AP(w) := \frac{180}{\pi} \arg\left[\frac{2}{1 + (j w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right]$$

Half Ckt transfer function

$$HP(w) := \frac{180}{\pi} \arg\left[\frac{1}{1 + (j \cdot w)^2 \cdot L \cdot C + \frac{2 \cdot j \cdot w \cdot L}{R_{Load}}}\right]$$


Frequency Response of Output Filter
Amplitude [dB]
10
5
0
−5
−10
−15
−20
−25
−30
−35
−40
−45
−50
−55
−60
−65
−70
10
100
1·10^3
1·10^4
1·10^5
1·10^6
Frequency [Hz]
Full Bridge
Half Bridge


Frequency Response of Output Filter
Phase [deg]
45
0
−45
−90
−135
−180
−225
−270
10
100
1·10^3
1·10^4
1·10^5
1·10^6
Frequency [Hz]
Full Bridge
Half Bridge