



# Design Document

## SCR Box 2003

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### Abstract:

From May through September 2003, new SCR boxes were designed and constructed to replace existing boxes used in ECE469, Power Electronics Laboratory. The old boxes were fully analog and required frequent calibration in order to perform properly. The new boxes use digital timing and have a host of new features to enable their use in advanced experiments, both for teaching and research use.

Document Revision History

Issue	Date	Comments
000	02/12/04	Released after revision and review.
001	9/15/04	Integrated contents of DOC00001-000 (test procedure)

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## 1. Introduction

This project provides advanced SCR systems capable of being used in a multitude of projects. Jonathan Kimball is the project manager, mechanical designer, and power designer. Zakdy Sorchini is the digital and analog designer and the software engineer. Construction assistance was provided by Yongxiang Chen, the ECE Electronics Shop, and the ECE Machine Shop.

### 1.1 Scope

The primary end use of the boxes is for ECE369 use. Therefore, it must be rugged and reliable in an undergraduate lab setting. It must also be easy to debug and repair.

In addition, it is desirable to provide advanced capabilities used in a research setting. This includes operation from an external trigger ranging 50-400 Hz, and either time-based or PLL-based angle determination.

The box contains three SCRs, for phases A, B, and C.

### 1.2 Definitions

Master delay: time or pulse count from rising edge of master trigger to the initiation of phase A firing.

Phase-to-phase delay: time or pulse count from the initiation of phase A firing to initiation of phase B firing, and from initiation of phase B to initiation of phase C.

### 1.3 References

Schematics: SK0009 rev 1 and SK0010 rev 3

Layouts: PB0009 rev A and PB0010 rev B

Drawings: [PJ0004 rev B](#)



## 2. Core Timing Design

A digital timing design provides more flexibility and allows repeatability of experiments, since specific delay numbers can be dialed.

The principle behind timing is very simple: the main trigger signal (generated from the internal or external trigger circuit) starts the process by enabling a counter which counts up to the specified delay and then activates a “done” signal and also enables the next counter. In the actual design the timing process is regulated by a microcontroller PIC16F72 from Microchip and a XC9572 CPLD from Xilinx. Most of the timing circuit is implemented in the CPLD.

### 2.1 Microcontroller Timing

The microcontroller is used to obtain the delay (master and phase-to-phase) information from the user via the encoder interface and load the counters when it is safe to do so.

#### 2.1.1 Delay Information

To obtain the delay information from the encoder input, the  $\mu\text{C}$  is assumed to be fast enough to be able to scan the encoder inputs to detect any change. Each cycle the  $\mu\text{C}$  reads the encoder value along with the MASTER/PHASE switch state to modify the proper register. A brute force approach is used to update the delay register, namely, the encoder value is compared to a previous value and the appropriate action is taken (i.e., increase or decrease the register). The code assumes that the encoder will not jump more than one state between reads; if that happens, no register is actually modified.

Additionally, there is a calibration delay DIP switch, SW1, which allows an extra delay to be added to the master delay. The  $\mu\text{C}$  is also responsible for reading this value and adding it to the master delay.

#### 2.1.2 Counter Loading

The delay values are loaded into the corresponding counters after they reached the zero count and are inactive. When a counter is done, it triggers an interrupt on the  $\mu\text{C}$ , which then loads that same counter with the proper value.

### 2.2 CPLD Timing

Once the counters are loaded, they are ready for the timing sequence. Internally, a flip-flop is activated when the positive edge of the trigger signal occurs, which starts the counting process and signals a “count in progress” state for the Master Delay counter. When the count reaches zero, the flip-flop is deactivated and the next stage’s flip-flop is activated, which starts a similar process. The same occurs for the third stage.

As mentioned in the previous section, the  $\mu\text{C}$  responds to the “counter done” event via an interrupt process. The  $\mu\text{C}$  then enables a pulsing signal that is fed into the CPLD, one for each corresponding counter. These three signals along with the “count in progress” signals are used in an AND array to generate the SCR pulses for each phase. Additionally, a global Master Enable signal ANDs with the SCR pulses for a global enabling capability.



The CPLD timing implementation also covers a trigger signal deglitching circuit, which is able to remove false positive edges from the trigger signal. False edges are generated by the load circuit when turning on an SCR, or when commutating current. These are primarily observed on the external trigger circuit, since the internal trigger stage lies behind the power transformer of the box. The circuit uses a flip-flop to disable subsequent triggering which is reset before the next true edge comes in.



## 3. Power Circuit Design

The power circuit consists of four main parts: power supply, internal and external trigger generation, SCR gate firing, and the actual SCRs.

### 3.1 Power Supply

The power supply is a simple linear supply derived from a 120V:12V center-tapped transformer, shown on page 7 of SK0010. Each half of the secondary is half-wave rectified, to yield an approximately 17V DC source. Linear regulators, an LM7812 and an LM7805, are used to derive voltages used in the rest of the circuit. The 12V supply is only used by the SCR gate firing circuits, but also serves as the source for the LM7805. The 5V supply is used for the remainder of the circuitry. There are additionally resistors separating digital and analog supplies.

The total current required by the circuitry is approximately 1 A. This results in high power dissipation in the linear regulators. Clip-on heat sinks are used, Wakefield 574502B03300 with the mounting tabs clipped (Digi-Key HS220-ND). These are sufficient to keep case temperatures below 85°C in a closed box in a 22°C ambient under all load conditions up to 10 ADC from a 208 VAC source.

### 3.2 Trigger Generation

#### 3.2.1 Internal Trigger

There are two trigger circuits. The first is derived from the power supply transformer. It is used in the teaching laboratory. The circuit is located primarily on page 10 of SK0010, fed from the power supply on page 7. The capacitor shown, combined with the parasitic inductance and resistance of the transformer, filters out any noise on the line. U10, a 2.5V reference, is used to move the zero crossing circuit away from ground. This is necessary because of the single-supply topology chosen. A small amount of positive feedback is necessary due to the slow nature of the power feed (60 Hz).

#### 3.2.2 External Trigger

The external trigger is derived from a 12-120 VAC source. For example, the laboratory benches include a 25 VAC line-to-neutral single- or three-phase source, which can be fed into the external trigger. For more sophisticated experiments, if line-to-neutral voltages are less than 120, they can be used directly; otherwise, a simple transformer can be used to derive an appropriate voltage.

The external trigger source may be at any potential with respect to ground, so full isolation is needed. For simplicity of the power supply, the necessary power is derived from the external trigger source itself. It requires approximately 20 mA. This is shown at the upper left of page 11 of SK0010. The TIP47, 1N4744, and R32 combine to make a rudimentary linear regulator. It is fed from half-wave rectified voltage via D15. There is no capacitance at the input, because that would require the linear regulator to continuously drop a high voltage. Instead, the rectifier capacitance is located after the linear regulator. The result is significant ripple in “+V”, but the remainder of the circuit is tolerant to the ripple.



The zero crossing circuit is essentially identical to the internal trigger circuit. To keep current consumption down, some values are changed. An RLC filter was found to be necessary to prevent glitches on the trigger signal when using the 25 VAC line-to-neutral source for both triggering and load. This reduced line notching enough that the glitches could be handled in software.

Unfortunately, the filtering adds delay, on the order of 100  $\mu$ s. For each box, the delay is measured and recorded.

To complete the isolation, an optocoupler is used, shown at the bottom of page 10 of SK0010.

### 3.2.3 Coordination

There are two switches and a jumper involved in complete coordination of the internal and external trigger. First, there is a jumper to invert the nominal internal trigger, in case of an error in wiring, etc., J5 on page 7 of SK0010. Next, there is a switch connected to J7 on page 10 to choose internal or external triggering. Finally, there is a switch connected to J8 on page 10 to give true or inverted operation.

Typical operation in the teaching lab is to derive the power from (plug the box into) phase A of the source that you are controlling. J5 is in the "NORM" position, J7 is in the "INTERNAL" position, and J8 is in the "TRUE" position. For two-box experiments, such as for a full bridge rectifier, one box would have J8 in the "INVERTED" position.

### 3.3 SCR Gate Firing

There are three gate firing circuits for the three phases, shown on pages 2-4 of SK0010. References to follow are for phase A on page 2.

R8 sets the gate current. The voltage across the primary of T2 is given by the gate-cathode drop plus a small drop in R4, plus a diode drop in D1. The source is a regulated 12V. R8 is chosen as 100  $\Omega$  to set the current at approximately 100 mA, assuming all of the drops on the secondary add up to 2 V.

D9 is a flyback diode and D6 provides flux reset. Values are chosen so that the flux always resets after every pulse, even for worst-case on-time. The transformer is a Coilcraft SD250-1. R1 and C1 form a gate snubber, possibly unnecessary but always advisable.

### 3.4 SCRs

The chosen SCRs are International Rectifier 10RIA40 stud-mount non-isolated devices. All three are mounted to a single heat sink, Wakefield 403K. Isolation is achieved with thermal washers. Additionally, there are O-rings on the studs to guarantee separation between the stud and the heat sink.

The SCRs have been tested using a 208V three-phase source in a mid-point rectifier with a resistive load up to 10 ADC. They have also been tested with RL loads and capacitive loads from lower voltages. The highest case temperature seen is 56°C in a 22°C ambient with the box closed. It is anticipated that even higher currents are possible without stressing the SCRs.



## 4. User Interface

Any piece of equipment is useless without a good user interface. Most of our inputs as well as the display are on the front panel of the box. The external trigger and the internal/external switch are on the back, putting them out of sight (and hopefully out of mind) for the novice user.

### 4.1 Timing Control

There are two displays integrated on PB0012. The display was originally calibrated in pulses, but now displays in milliseconds, in increments of 5 ms. Each display unit is a four-digit seven-segment LED. They are labeled “master” and “phase” for master delay and phase-to-phase delay.

The user input for fully digital operation is an encoder. We chose a Grayhill 62A11-02-050S optical encoder for reliability; it includes mechanical detents for tactile feedback. For long delay times, incrementing in 5 ms steps would be interminably slow, so a coarse/fine switch is available. In coarse mode, increments are 100 ms. Another switch determines whether the user is adjusting the master or phase-to-phase delay.

For some applications, an analog input is desired. This allows the construction of a closed-loop system. A switch determines whether the master delay derives digitally or from the analog input. The analog input is a BNC with a 50 ohm termination and protection. The input range is 0 to 5 V, which corresponds to a delay range of 0 to 20.47 ms.

### 4.2 Operational Control

At power-up, delays are all set to minimum (0.005 ms for master, 0.300 ms for phase-to-phase) delay. To give the user the opportunity to adjust delays prior to energizing the power circuit, an enable switch is available.

Standard operation fires the A phase SCR some delay time after the master trigger goes high. In some applications, such as the negative half of a bridge rectifier, the user may desire to fire after the master trigger goes low. A “TRUE/INVERTED” switch is available for this operation.

Advanced users may desire external triggering. The switch towards the bottom of the back panel is an internal/external switch. The master trigger goes high when the voltage on the orange post goes positive with respect to the blue post.

There is a power switch on the back panel. Power derives from a standard IEC320 cord via a 250 mA standard fuse. Power is indicated by an LED on the front panel, which is powered from 5V.

### 4.3 Power Connections

The SCR anodes and cathodes are on the front panel via binding posts. Each is rated for 15 A. Orange is the anode, for a weak “positive” connotation.

### 4.4 Internal Jumpers

A jumper, J5, is provided to invert the main internal trigger. This may be necessary depending on how the rest of the box is wired. So far, we have not needed to invert.





A jumper, JP2, is provided to switch from the microcontroller-derived clock to a PLL-derived clock. This can be used for other frequencies besides 60 Hz. For proper operation of the PLL, another jumper, JP1, is provided to set the nominal center frequency of the oscillator. The high range is for 400 Hz, the low range is for 50/60 Hz, and the middle range is for other frequencies in-between. Note that in PLL operation, the displayed delay will be  $0.005x$  the number of pulses, with 4096 pulses per cycle.



## 5. Enclosure Design

The enclosure is a modified Hammond 1458E5. We chose ASA 61 Grey for the top and bottom, and stayed with the standard Contempra Gray (more like beige) front and black back. This type of box was chosen to be consistent with the 2002 version of the FET box.

The enclosure was designed in Autodesk Inventor. PDFs of the machining prints are available, as well as the source Inventor files, under PJ0004 rev B.

The front panel was silk-screened black. At the time the order was submitted, we planned to have the display in pulses. We later decided to display milliseconds to reduce confusion. The ECE Machine Shop painted over the text indicating the readout type.

Looking back, the box is really just a little too small for the system. It would have been better to have another inch in height and in width, although depth would not have helped much. The 1458E5 gave us the best possible solution for a standard box. The height is dictated mainly by the SCR heat sink assembly, but also by the display board and binding posts on the front panel. The width is dominated by the SCR heat sink assembly plus the power outlet and switch. Another inch in width would have greatly simplified the assembly of the power input.



## 6. Test Procedure

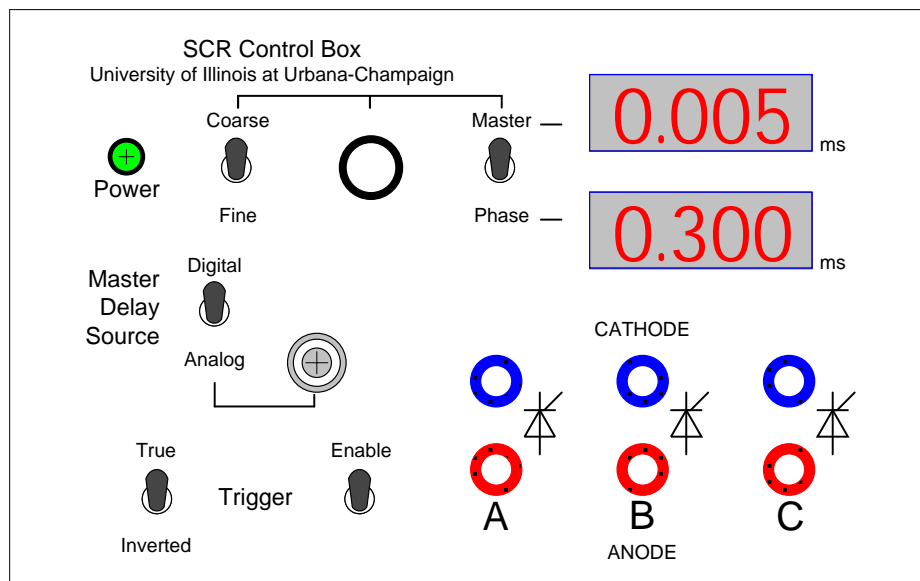
### 6.1 Preface

This test procedure was meant to be as generic as possible, but a couple of issues specific to the Power Lab at the University of Illinois could not be made generic enough:

- It is assumed that a 120 V<sub>AC</sub> three-phase set (standard plug) is available to power equipment and is synchronized to whatever three-phase source is used in the experiments.
- Some steps require the use of a 25 V<sub>AC</sub> (**line to neutral**) three-phase source. Transformer implementation of this source should have a Y-connected secondary at a low enough potential to be safe for testing, but high enough to be able to power the external trigger circuitry. Refer to 3.2.2 for the proper ratings.

### 6.2 Introduction

The added complexity of the new SCR Boxes requires a systematic test procedure. This section allows any user to verify operation of the box, either after initial assembly or for troubleshooting. Individual subsections cover testing of the different subsystems of the SCR Box. For reference, a diagram of the front panel is shown in Figure 1.



**Figure 1. SCR Box front panel diagram.**

The trigger source selector switch is located on the back panel. The position TOWARDS the external trigger banana post connectors is for external triggering. Similarly the position AWAY from the connectors is for internal triggering. The orange terminal is positive relative to the blue terminal.



All measurements, unless otherwise stated, are referenced to ground. Ground test points available are TP12, TP14, TP21, TP22 and TP23. Analog ground is TP18. The isolated ground for the external trigger input is TP44. As a reference, Figure 2 shows a diagram of the main board to aid in locating individual parts or test points.

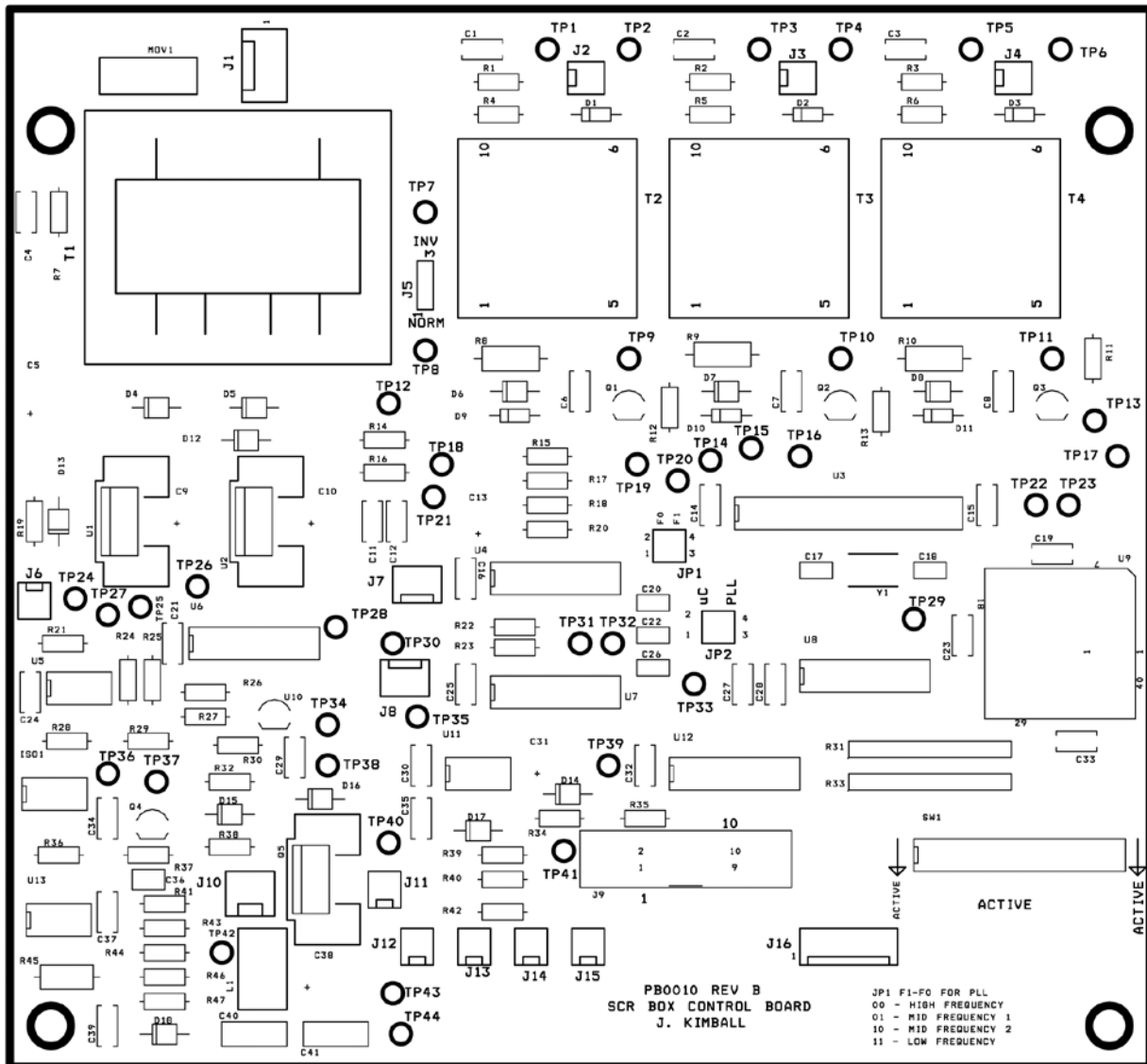


Figure 2. SCR Box control PCB diagram.

### 6.3 Known Issues

- Noise is injected to the digital bus line from the serial clock within the interface cable that connects the main PCB to the display PCB. This problem will manifest itself as random firing of the SCRs, and seems to be more sensitive as the master delay is increased. A workaround is to use a custom interface cable that shields the lines and uses an overall shield. The particular grounding scheme (on each side or both sides) did not seem to make any difference, but in general it was observed that this solution minimizes the problem.



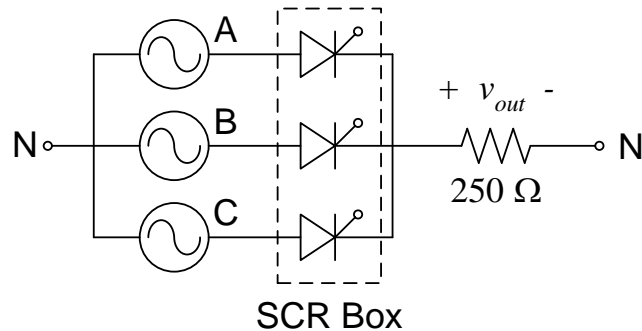
- The accuracy of the delays is limited ( $\pm 5 \mu\text{s}$ ) by the uncertainty created from the lack of synchronism between the high frequency clock derived from the microcontroller and the trigger signal derived from the internal or external trigger circuit. Although the high frequency clock derived from the PLL section is synchronized to the trigger signal, the resolution of the PLL itself (since it is working as a frequency multiplier) also gives a comparable uncertainty. Reduction of the multiplier (current implementation uses a  $2^{12}$  multiplier) should minimize this uncertainty.
- When using the external trigger, noise in the input voltage (particularly spikes) can alter the zero crossing detection or introduce false triggering. A passive filter is used to minimize the effect of this noise. This has the effect of introducing a delay (about  $100 \mu\text{s}$ ) in the trigger signal. Noise spikes are particularly troublesome and are typically created by current commutation. Therefore, the trigger logic is designed to remove false triggers once the trigger sequence is already in progress. Essentially the zero crossing detection is disabled during particular periods in time when a true zero cross cannot occur.

## 6.4 Converter Operation

This section covers the tests that do not require opening the SCR Box for access to internal signals. It should be used to verify normal operation of the box. Typical failures for this section are missed phases at the output (SCR not fired or bad internal connection), no output (problem with True/Inverted switch or with trigger circuit), improper phasing or wrong delay observed (mixed internal SCR connections, problem with True/Inverted switch or misconfiguration of the internal calibration delay).

1. Connect the power cable of the box to the phase A power outlet.
2. Connect phase A (typically from the  $25 V_{AC}$  source) to the external trigger. The phase wire should be connected to the orange connector and the neutral to the blue connector.
3. Power up the SCR Box. The main power LED should light up and the displays should read 0.005 for the Master delay and 0.300 for the Phase-to-Phase delay. If the box does not power up or the displays do not light up, verify operation of the power distribution. Sometimes, the displays might power up with all segments illuminated. Turning the box off and on should correct the issue; if not, there is a problem with the display.
4. Set the Phase-to-Phase delay to 5.555 ms (the nominal value for 60 Hz operation).
5. Implement a half-bridge controlled rectifier as shown in Figure 3, using the  $25 V_{AC}$  source (the 3-phase transformer set). Connect the differential (scope) probe across the load resistor. Setting the scope's trigger to AC line will help displaying the waveforms.

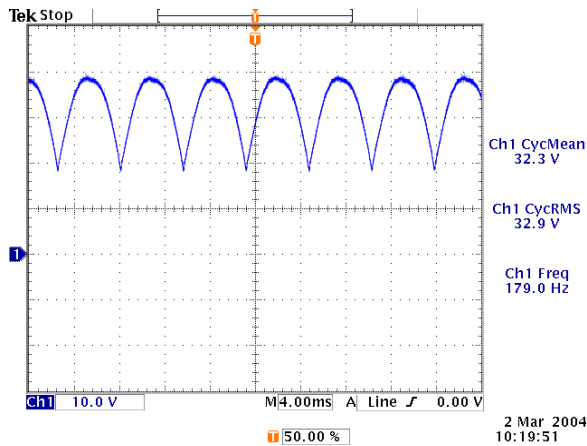




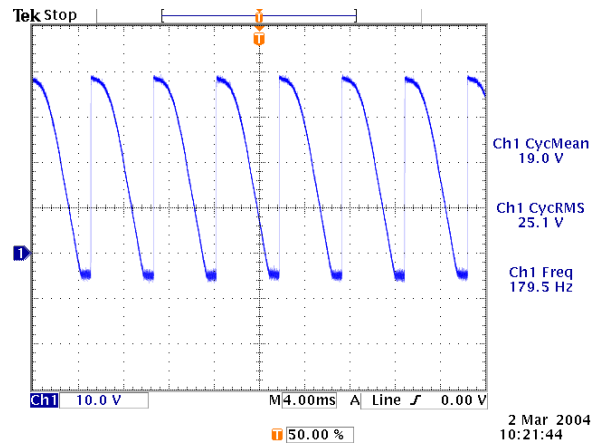
**Figure 3. Half-bridge controlled rectifier with resistive load.**

6. Set the trigger switch to Internal.
7. Verify operation of the (trigger) Enable switch. Enabled will show a waveform similar to what is shown in Figure 4. Disabled will make the output of the converter zero.
8. With the Master delay control set to digital, vary the master delay from 0.005 ms to about 9 ms using BOTH the coarse and fine control to verify their operation. The output should look like the sequence shown in Figure 4. If the waveform does not resemble the ones shown in the figure, verify operation of the trigger stage.
9. Set the trigger switch to External.
10. Verify operation by repeating steps 7 and 8. The waveforms should be almost the same.
11. Connect a function generator to the BNC connector for analog control. Set the function generator for a sine wave of 1 Hz between 0 and 2 V.
12. Set the Master Delay Source to Analog (use any trigger source). This will modulate the delay by the sine wave. The modulation should be close to 100 % (i.e., the delay should go from about 0 ms to 9 ms giving 100 % to 0 % output voltage). The modulation process in a slow time scale should look like what is shown in Figure 5. If the output is not modulated, then verify the analog input circuit (User Interface Section).

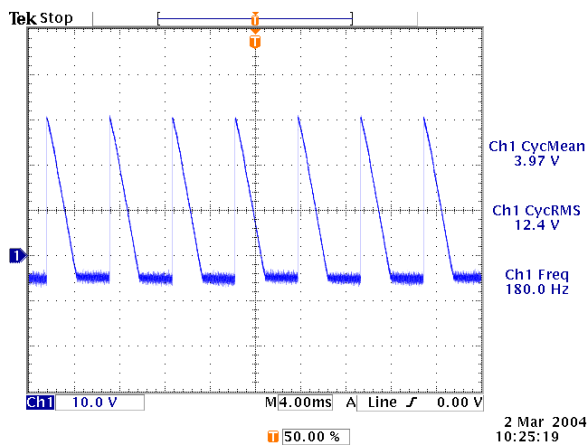




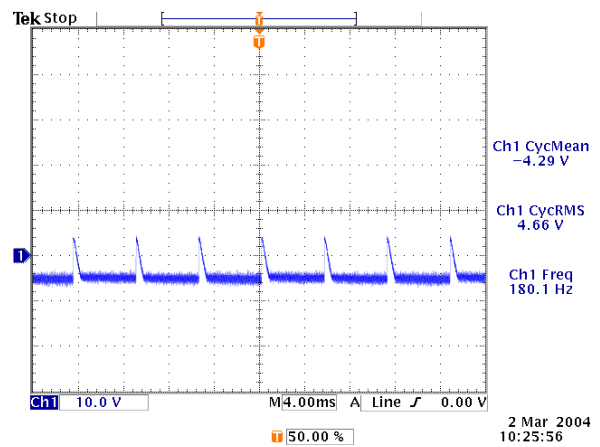
(a) 0.005 ms



(b) 4 ms



(c) 6 ms



(d) 8 ms

**Figure 4. Converter output for different Master delays.**

13. Verify operation of the True/Inverted switch. Reverse the connections on the external trigger input and set the switch to Inverted. Operation should be the same as in step 8, since the reversal of the external trigger connections is cancelled by inverting the trigger.
14. If no faults are found, the box is functioning properly; terminate the test.



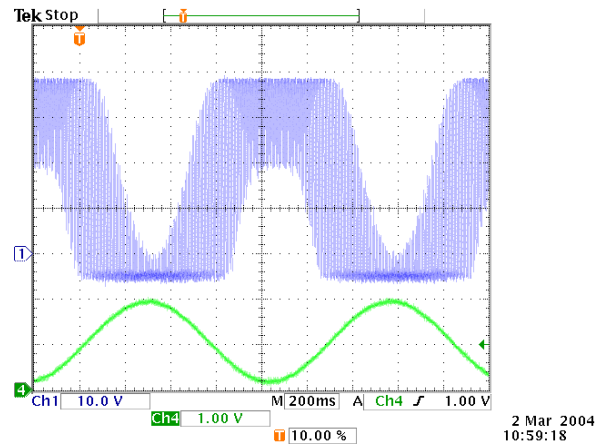


Figure 5. Output voltage modulation.

## 6.5 Power Distribution

1. Connect the power cable to any electrical outlet and power up the box. Verify that the Power LED lights up and that the LED digits light up (they should light up as 0.005 for the Master delay and 0.300 for the Phase-to-Phase delay).
2. Verify that ac power is available. Connect at TP8 and at TP7; and verify that the readings are equal and around 14 V<sub>RMS</sub>. If no voltage is present, check the fuse on the power receptacle.
3. Verify the dc power voltages. TP24 should be unregulated 16 V, TP25 should be 12 V nominal, TP26 should be 5 V nominal, and TP28 with respect to TP18 should be 5V nominal.
4. Verify dc power to the display board mounted on the front panel. If the voltages on the main board are correct and the displays light up as 0.005 and 0.300, then power is ok. Otherwise, verify that pin 6 on the display board is 5 V nominal. Alternatively, the terminals toward the inside of the board on R1 or C1 can be verified.

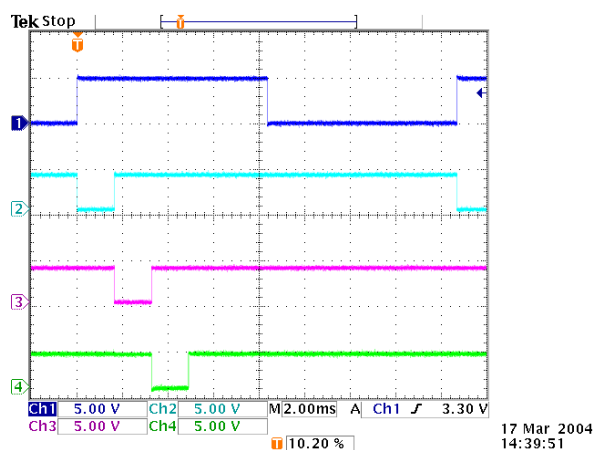
## 6.6 Trigger System

1. Make sure that the calibration delay (SW1) is set to zero (all jumpers inactive). The inactive position (as marked in the board) is AWAY from the front panel.
2. Follow the procedure in Part 1 to prepare the box for normal converter operation. Monitor the output voltage with the differential probe.
3. Verify the operation of the microcontroller. Check TP29 for the high frequency clock at a nominal 200 kHz (NOT 50 % duty ratio). If this signal is not present then the microcontroller is not operating properly.
4. Verify the internal trigger circuit.
  - a. Verify that TP38 is fixed at 2.5 V nominal (voltage reference).
  - b. Verify that TP27 is a square wave at nominal 50 % duty ratio and in phase with the voltage powering the box (typically phase A).

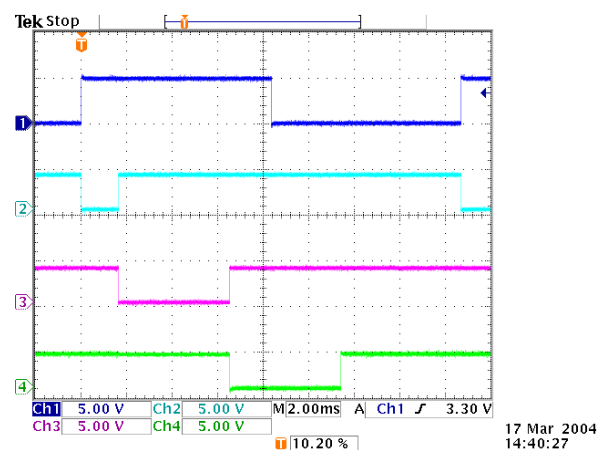




5. Verify the external trigger circuit. Use the differential probe when verifying signals on the isolated side.
  - a. Using the isolated ground (TP44), verify that TP43 is approximately 13 V unregulated dc.
  - b. Verify that TP42 is 5 V nominal (zener regulated).
  - c. Verify that TP37 is a square wave at nominal 50 % duty ratio and in phase with the external trigger input voltage.
  - d. Verify that TP36 shows LOGICAL inversion of the previous signal (the signals will have different amplitudes). This is on the output side of the optical isolator, so a regular probe can be used.
6. Verify TP35, the main trigger signal going into the CPLD. This is the trigger signal according to the trigger source selector and the True/Inverted switch. Verify all combinations of both switches (no change should be observed between internal and external triggering). Keep the signal in the scope as a reference.
7. Verify TP33, the high frequency clock going into the CPLD; it should be the same as TP29. Make sure that JP2 is closed to gate the high frequency clock coming from the microcontroller.
8. Verify the master counter enable signal, EN\_MC (TP15, active low). Move the signal with signal by changing the Master delay. The falling edge should be in synch with the raising edge of the trigger signal. The raising edge should move as the Master delay is varied. Refer to Figure 6 (Ch1 – Trigger, Ch2 – EN\_MC, Ch3 – EN\_PPC1, Ch4 – EN\_PPC2).
9. Verify the phase-to-phase counter 1 signal, EN\_PPC1 (TP16, active low). The whole signal should move as the Master delay is changed. The raising edge should move as the Phase-to-Phase delay is varied. Refer to Figure 6.
10. Verify the phase-to-phase counter 2 signal, EN\_PPC2 (TP20, active low). The whole signal should move as the Master delay is changed. Both edges will move as the Phase-to-Phase delay is changed. Refer to Figure 6.

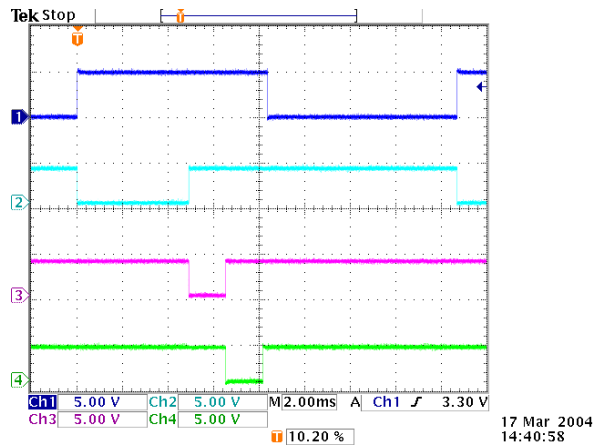


(a) Master delay 2 ms, Phase-to-Phase delay 2 ms

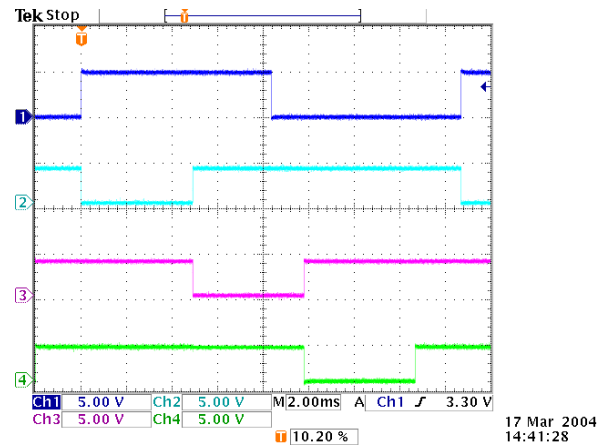


(b) Master delay 2 ms, Phase-to-Phase delay 6 ms





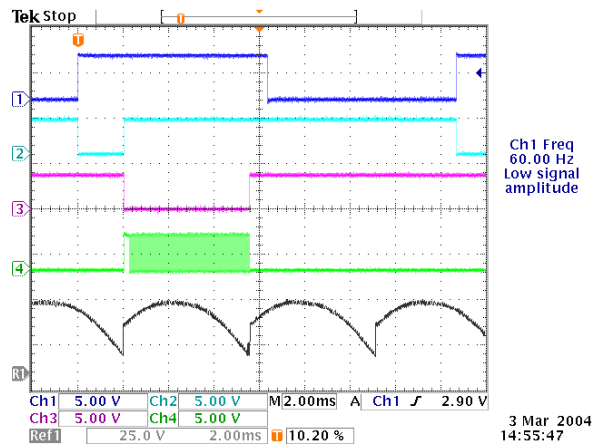
(c) Master delay 6 ms, Phase-to-Phase delay 2 ms



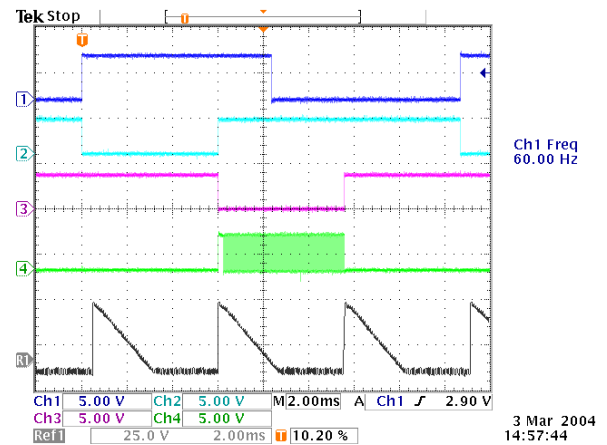
(d) Master delay 6 ms, Phase-to-Phase delay 6 ms

**Figure 6. Timing sequence for different delays.**

11. Set the Phase-to-Phase delay to 5.555 ms (nominal for 60 Hz operation) and enable SCR firing.
12. Verify the gate control signals for the SCRs, TP19 (SCR A), TP17 (SCR B) and TP18 (SCR C). They should be pulse trains that start with the raising edge of the corresponding enable signal (SCR A – EN\_MC, SCR B – EN\_PPC1 and SCR C – EN\_PPC2) and end with the falling edge of the next one. Figure 7 shows the sequence to be expected for Phase A, for Master delays of 1 ms and 6 ms. Ch1 is the trigger signal; Ch2 is EN\_MC, Ch3 is EN\_PPC1; Ch4 is the SCR A control signal; and Ref1 is the output voltage waveform. Notice that the first pulse of the SCR control signal is wider.



(a) 2 ms



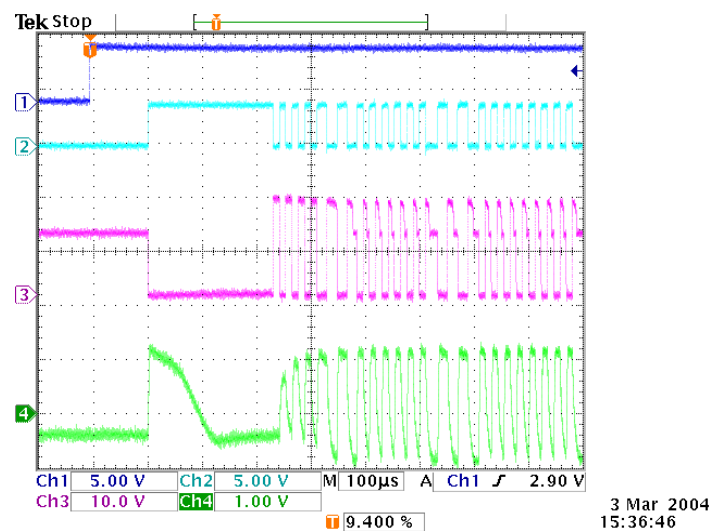
(b) 6 ms

**Figure 7. Phase A trigger sequence for different Master delays.**

## 6.7 Gate Drives



1. From 6.6, SCR control signals should have been verified. These are the pulses that are fed to the gate drives.
2. Verify the voltage on the primary side of the pulse transformer for SCR A (TP9). It should be at 12 V at rest and pulse between 0 V and 28 V when active. If flux is completely reset during pulsing, the signal goes back to 12 V.
3. Connect the differential probe across TP1 and TP2, the secondary side of the transformer. This is the voltage applied to the gate of the SCR. The secondary voltage should mimic the primary voltage. Figure 8 shows the gating process for a small Master delay. Ch1 is the trigger signal, Ch2 is the control signal, Ch3 is the primary side voltage and Ch4 is the voltage applied to the gate of the SCR.
4. Repeat the previous step for SCRs B and C primary side (TP10 and TP11) and the corresponding secondary voltage (TP3, TP4 and TP5, TP6).



**Figure 8. Gate drive A operation for a small Master delay.**

## 6.8 PLL Section

The SCR Box includes a PLL section as a second source of high frequency pulses that feed the counters in the delay process. By synchronizing to the trigger signal (internal or external) the delay is in degrees as opposed to absolute time. Therefore, a fixed delay can be achieved (i.e., delay angle  $\alpha$ ) independently of the frequency of the power source. A multiplier of  $2^{12}$  is used, thus giving a resolution of approximately  $0.088^\circ$  per step.

The high frequency clock generated by the circuit has to be manually selected (JP2) to be used in the trigger circuit.

1. Make sure that the frequency range of the circuit is correct. Typically it will use the low frequency range (i.e., both jumpers in JP1 closed) for 60 Hz operation.
2. Verify the signal in TP31. This should be in synch with whatever the trigger signal is (i.e., Internal/External, True/Inverted). If it is not (assorted notches on the signal jumping around), then the frequency range might not be correct.

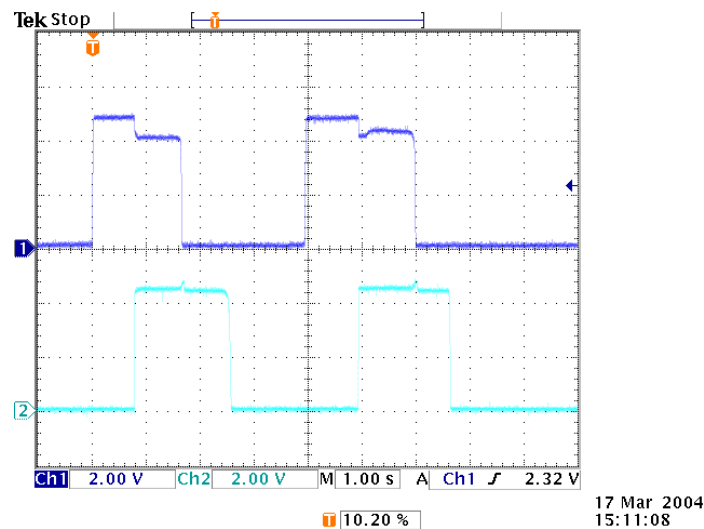


3. Verify the signal in TP32. This is the high frequency clock generated by the circuit and should be nominally  $2^{12}$  times the input frequency (245.7 kHz for 60 Hz input).

## 6.9 User Interface Section

This section covers the analog input and the encoder logic. The analog input has a  $50\ \Omega$  input impedance, so the source driving this input should not be soft. The outputs of the encoder are open collector, so pull-up resistors are used.

1. Verify TP41 and TP39 for proper operation of the encoder. They should be square waveforms that follow a repetitive pattern as the encoder is moved (every four steps the sequence will repeat). Figure 9 shows the sequencing of the encoder outputs as the encoder is moved eight steps (two cycles); each step corresponds to a particular logic combination of the encoder outputs (Ch1 – TP41, Ch2 – TP39). If no signal is present, there is probably no power feeding the encoder.



**Figure 9. Encoder outputs for a two cycle movement of the encoder.**

2. For the analog input, if no control of the Master delay is achievable, one of the input protection diodes might be damaged or reversed.
3. Verify the physical integrity of the MTA-100 connectors. During assembly it was observed that a significant number of connectors were not crimped correctly and therefore bad connection to the header resulted. Also, sometimes the switches on the front panel might fail.

